SIEMENS

SIPROTEC 5 Application Note

Circulating Current High Impedance Differential Protection Using 7SJ8

SIP5-APN-030, Edition 1

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Content

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SIPROTEC 5 Application Note

1 Circulating Current High Impedance Differential using Multifunctional Relay 7SJ8

1.1 Introduction

This application note describes the multifunctional relay SIPROTEC 7SJ8x used in high impedance protection applications.

Three-phase (phase-segregated) circulating current high impedance protection schemes are typically applied for the following protection objects: busbars, auto-transformer, series reactor, shunt reactor or even to motors or generators. Regarding busbars arrangements, the high impedance protection scheme is widely used for arrangements like single busbars, single busbars with sectionalizer, or circuit-breaker-and-a-half arrangements. The usage of high impedance busbar protection for double busbars is not recommended, because of high complexity related to switching-over of CT secondaries that decreases the scheme reliability.

Single-phase restricted earth fault (REF) protection schemes may be used in principle to all the protected object as listed above, but the most common application is to protect transformer windings which are earthed via impedance, solidly earthed or even for transformer winding connected in delta (in this case the scheme is sometimes called high impedance balanced earth fault).

The multifunctional relay SIPROTEC 5 7SJ8x can be used within all the mentioned high impedance protection schemes, both in phase-segregated circulating current high impedance protection applications, as well as in single phase restricted earth fault protection applications.

This document provides description of the multifunctional relay SIPROTEC 5 7SJ8x application in phase-segregated circulating current high impedance protection scheme. Thereby the guideline for the calculations related to the high impedance differential protection schemes is described together with the comments on the relay setting parameters.

1.2 Circulating Current High Impedance Protection

1.2.1 General information of High Impedance Protection Schemes

In contrary to the low impedance differential protection schemes, where each of several CTs forming differential protection zone is directly connected to a separate relay input, the high impedance protection scheme is formed by the parallel connection of all CTs secondaries within a given protection zone (Figure 1).

While low impedance protection schemes evaluate signals within the relay that come from each of the CTs independently, the relay in the high impedance scheme evaluates the current that results from the interaction of all the involved CTs as it flows in the differential branch (Figure 1).

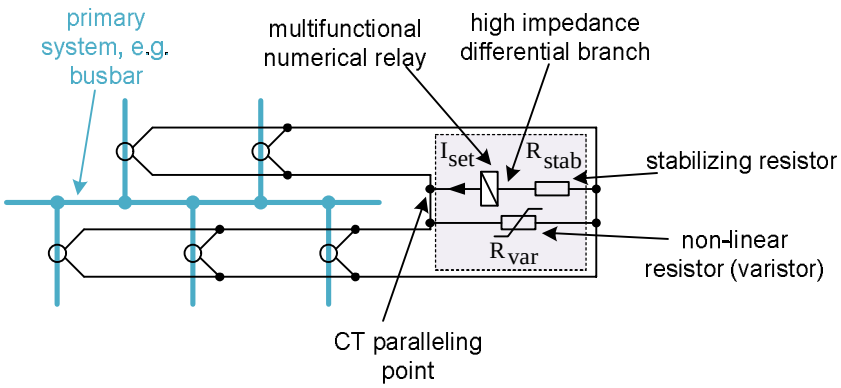


Figure 1 Typical connection of elements within a high impedance differential protection scheme.

Thereby, the stability of the differential scheme on CT saturation plays in all schemes an important role.

Low impedance protection schemes evaluate CT secondary currents which may be saturated by their high burden and/or high secondary currents. Thereby, multiple CT currents are evaluated by relay (nowadays relay software), whereas each CT saturates independently from the others, i.e. the CTs do not influence each other in their performance. Therefore, in the low impedance differential protection devices several different stabilizing measures and algorithms for better stability and selectivity are applied.

Within a high impedance scheme the CTs do influence each other, as all of them are connected in parallel (Figure 1). The stabilization against CT saturation is realized by the placement of an extra element (hardware), namely the stabilizing resistor so no further measures against CT saturation have to be implemented in the relay. Therefore, the relay used within the high impedance protection scheme can be of over-current relay type without involving any additional measures against CT saturation. All the other high impedance scheme performance quantities: as required fault sensitivity, scheme stability are then dependent on the scheme design involving adequately chosen CT parameters and auxiliary components (stabilizing resistor, varistor) that suit given application.

1.2.2 High Impedance Protection Scheme Design

1.2.2.1 Relevant primary system data

Protection object characteristic has major influence on the protection scheme design. Therefore, typically the following properties shall be known

- Short-circuit fault level including:
  - maximum symmetrical short-circuit withstand current of the switchgear
  - maximum symmetrical short-circuit current for external (through) faults
  - maximum symmetrical short-circuit current for internal faults
  - minimum symmetrical short-circuit current for internal faults

For the later ones especially neutral earthing conditions (earth-fault limitation) shall be considered, as well. Moreover, all the above currents can be three-phase, double-phase or phase-to earth depending on the application/protected object.

- Rated parameters of the protected object including
  - rated power, resp. rated current, impedance voltage, sub-transient reactance, ...
- Rating of the primary switching elements like circuit breaker, isolators within the switchgear that are relevant to the protected object

1.2.2.2 Relevant current transformer data

The prerequisite (a must) to high impedance schemes is that all the involved CTs have to have the same current ratio. The usage of CTs as per IEC 61869-2 Standard [1] class PX (former BS class X) is generally recommended. Those CTs have current ratio error limitation and are of low-leakage type. However, for some high impedance protection schemes involving less number of CTs (e.g. REF) also CT of IEC 61869-2 class 5P can be used. Thereby, their current ratio error as well as the respective magnetizing curves together with internal resistances shall be known. Also CTs of the former (now obsolete) IEC 44-6 class TPS can be used within high impedance protection applications.

[1] Definition as per IEC 61869-2; in practice the term 'knee point voltage' is widely used for this quantity. However, as per standard the term knee point voltage describes rather the voltage that is applied to the secondary terminals of the CT during testing. For the sack of the standard compatibility and correctness the term emf will be used through this application guide.

Hereby, it is recommended to transfer their nameplate parameters to the respective IEC class PX parameters. For high impedance busbar protection SIEMENS recommends usage of IEC class PX cores.

The following relevant CT parameters shall be known:

- CT nameplate data (preferably confirmed by test protocols)
- CT ratio
- CT knee-point electromotive force (emf)[1]
- CT exciting current at the knee-point emf
- CT secondary winding resistance at 75 °C
- CT secondary wiring resistance from the CT clamps to the paralleling point of the scheme (loop resistance)
- Number of CTs that belong to the differential protection zone

Remark: Regarding knee-point emfs, exciting currents and secondary winding resistances of the used CTs it can be stated that small deviations between the used CTs can be typically tolerated without negative influence on the scheme performance. The scale of deviation and its influence on the scheme design and performance, however, shall be analyzed on a case basis.

1.2.2.3 Relevant protection device data and auxiliary component data

For the high impedance scheme design the relay operating (settable) current range shall be known, so that it can suit the application with regard to the fault sensitivity. The burden of the relay input is typically very small comparing to external stabilizing resistance and can in most applications be neglected.

Remark: In the past the relays used constant operating current (e.g. 20 mA or 100 mA) and the setting was adjusted by settable resistors (mounted internally within the relay). Very often such relays were named 'voltage operated'. Nowadays, modern digital protection relay with wide range settable current setting are used. This gives additional flexibility for covering several high impedance protection applications using one type of the relay. The auxiliary component like resistors and varistors are then typically installed separately within the protection cubicle.

Further chapters guide on relevant calculations and propose scheme design for using multifunctional relay SIPROTEC 5 7SJ8x within high impedance differential protection schemes.

1.3 Procedure for High Impedance Protection Scheme Calculations

This chapter provides remarks on scheme design and a guide for the scheme relevant calculations.

1.3.1 Relevant required data

1.3.1.1 Establish the relevant power system data

At first the power system primary data that are relevant to the protected object shall be collected.

1. From the scheme stability and thermal design of components point of view the following relevant power system information shall be known:

- the maximum symmetrical short-circuit current for external (through) faults $I''_{sc,max,ext}$
- the maximum symmetrical short-circuit current for internal faults $I''_{sc,max,int}$

Remark: In case of a busbar, the maximum short-time symmetrical short-circuit withstand current of the switchgear $I''_{sc,max,swg}$ may be considered for both of the above quantities.

2. From the scheme sensitivity and relay setting range point of view the following relevant power system information shall be known:

- the rating of the feeder /diameter circuit breakers or maximum prospective load on those feeders $I_{r,load}$
- the minimum symmetrical short-circuit current for internal faults $I''_{sc,min,int}$

Remark: In power systems with solidly (effectively) earthed neutral-points, the double-phase fault is typically the smallest one and it can be typically considered here. In power systems with earth-fault current limitation (neutral point of power transformers is not directly earthed) the single-pole fault current shall be considered. However, for busbar protection schemes in networks with strongly limited earth fault current (e.g. to several Amps in medium voltage networks with presence of rotating machines) there is often not necessary to detect the earth- fault using such scheme.

1.3.1.2 Establish the relevant current transformer data

As previously mentioned the CTs used in the high impedance schemes shall be with equal ratios, of low leakage type and with limited current ratio error. For high impedance busbar protection SIEMENS recommends usage of IEC class PX CTs.

At first:

- the number of CTs that belong to the considered /designed differential protection zone N_{CT}

shall be known, and for each of these CTs their respective IEC class PX [1] parameters shall be collected :

- CT Ratio, $k_r = \frac{I_{pr}}{I_{sr}}$ where I_{pr} and I_{sr} are primary and secondary rated current, respectively
- rated CT knee-point emf E_k
- CT exciting current at the knee-point emf I_e
- CT secondary winding resistance R_{CT} (d.c. resistance corrected to 75 ^{O}C)

Remark: The values of knee-point emf and the respective exciting current can be obtained / read from the magnetizing characteristic or testing protocols. Both values shall be rms-values, as per IEC class PX.

Furthermore for each CT:

- the resistance of secondary wring from the CT clamps to the paralleling point of the scheme (loop resistance) R_{wire}

Remark: The wiring resistances are either given in the tender documentation or can be calculated from the layout drawings of the switchgear. Typically, a maximum wiring resistance can be estimated and specified as a maximum allowable for the worst case considerations.

1.3.1.3 Establish the relevant relay data and necessary auxiliary component elements

At first the relay relevant data shall be known:

- operating current setting range $I_{set,range}$,

- burden of the relay input used, typically expressed as resistance R_{relay} .

Regarding the first one, it is proposed to activate the following device configuration function in the multifunctional relay SIPROTEC 5 7SJ8x:

For 87B Hi application:

VI 3ph 1; 50/51 OC-3ph-B1, Definite–T 1

821.1941.661.1	Mode	on
_._.661.2	Operate & flt. rec. blocked	no
_._.661.8	Method of measurement	fundamental comp.
_._.661.3	Threshold (fault setting I_{set})	e.g. 0.5A Range: 0.03A ...100A, stps. 0.001A
_._.661.6	Operate delay	0.0 s Range: 0s ...60s, stps. 0.01s

Depending on application the Definite –T 2 stage can be used for CT supervision purposes or switched OFF in case when external supervision relay is used (this depends on customer practice).

VI 3ph 1; 50/51 OC-3ph-B1, Definite–T 2

821.1941.662.1	Mode	on
_._.662.2	Operate & flt. rec. blocked	no
_._.662.8	Method of measurement	fundamental comp.
_._.662.3	Threshold (superv. setting I_{superv})	e.g. 0.1A Range: 0.03A ...100A, stps. 0.001A
_._.662.6	Operate delay	e.g. oo (infinity) Range: 0s ...60s, stps. 0.01s

The actual burden of multifunctional digital relay SIPROTEC 5 7SJ8x can be taken from the relay manual (chapter technical data, 11.1.1):

$R_{relay} = 0.1\ \Omega$

11.1.1 Analog Inputs

Current Inputs

All current, voltage, and power data are specified as RMS values.		
Rated frequency f_{rated}	50 Hz, 60 Hz	
Protection-class current transformers	Rated current I_{rated}	Measuring range
	5 A	0 A to 500 A
	5 A	0 A to 250 A
	5 A	0 A to 100 A
	1 A	0 A to 100 A
	1 A	0 A to 500 A
Instrument transformers	5 A	0 A to 8 A
	1 A	0 A to 1.6 A
Power consumption per current circuit at rated current	Approx. 0.1 VA	
Thermal rating (protection and instrument transformers)	500 A for 1 s	
	150 A for 10 s	
	20 A continuously	
	25 A for 3 min	
	30 A for 2 min	
Dynamic load-carrying capacity	1250 A one half wave	

Furthermore, the relay SIPROTEC 5 7SJ8x requires always external equipment to build the high impedance protection scheme. This equipment consist typically of stabilizing resistor (-s) for setting up the respective scheme stabilization and non-linear resistor (-s) , i.e varistor (-s) to protect whole secondary equipment against overvoltages (i.e. CTs secondaries, the differential branch and the wirings). Typically per phase (per one relay input) one stabilizing resistor and one varistor is necessary.

The design and selection of these elements is subject of the scheme calculations (as shown in next chapters).

Remark: For busbar protection schemes which are equipped with CTs with high knee-point emfs, the presence of varistor is mandatory to protect the secondary equipment and wiring against high voltages that may appear during internal faults (see also calculations in item Error! Reference source not found.).

The presence of further relays e.g. for CT supervision, CT shorting, circuit breaker lock-out and/or test switches depends on respective customer practice.

1.3.2 Calculation of the minimum required stabilizing voltage

The prerequisite of a proper designed high impedance scheme is its stability to external faults. That means that protection relay installed in the differential branch must remain stable under maximum through fault conditions, when a voltage $U_{\text{diff,ext}}$ is developed across the differential branch due to high fault current and CT saturation.

This maximum prospective voltage $U_{\text{diff,ext}}$ can be practically calculated on a safe side assuming full CT saturation of one of the CTs within the scheme and considering the highest values of R_{CT} and R_{wire}. Taking the above into account, this voltage can be calculated as per Eq (1) and then taken as the minimum required stability voltage of the high impedance scheme U_{stab} :

$$U_{\text{stab}} = U_{\text{diff,ext}} = \frac{I_{\text{max,ext}}}{k_{\text{r}}}\left(R_{\text{CT}} + R_{\text{wire}}\right) \quad (1)$$

Remark: It is recommended that the differential branch is installed at the electrical mid-point of the system, i.e. the resistances R_{CT} and R_{wire} of all branches should be equal or similar. Slight deviations of R_{wire} can be typically tolerated but it must be kept in mind that these lead to an unbalance in the system during load conditions and in consequence may lead to an unnecessary energy dissipation (heating) at auxiliary scheme elements like stabilizing resistors. Also slight deviations of R_{CT} values between CTs used in a scheme can be tolerated. For most practical cases 'worst-case' value (highest R_{CT} among all CTs in a scheme) can be used in Eq. (1).

Summarizing, the setting voltage of the scheme U_{set} (in practice this voltage results from the multiplication of the relay current setting and stabilizing resistor value) over the differential branch must be made equal or greater than the required stability voltage (Eq. (1)).

$$U_{set} \geq U_{stab} \tag{2}$$

1.3.3 Calculation of the required fault setting

In further steps the following scheme requirements shall be assured:

a) the functionality (trip on internal fault) and
b) sensitivity of the scheme that suits given application.

Ad a): To assure the first requirement, the CT knee-point emf E_k shall fulfill the following requirement:

$$E_k \geq 2 \cdot U_{set} \tag{3}$$

Remark: Re-writing the Eq. (3)in form

$$U_{set} \leq E_k / 2 \tag{4}$$

and comparing it to Eq (2):

$$U_{set} \geq U_{stab} \tag{5}$$

one may become the minimum and maximum values for the scheme setting voltage. As per our practice it is worthy to keep in mind that the setting voltage U_{set} shall practically not exceed 300 V because this will introduce difficulties in finding the proper auxiliary equipment (like varistors, etc.).

Ad b): In order to reach the desired scheme sensitivity, i.e. to trip on internal fault, the current setting of the relay in the differential branch shall be calculated.

To do that, the desired primary fault sensitivity $I_{p,des}$ of the scheme shall be chosen at first.

The primary fault sensitivity, (i.e. the value of the primary internal fault current that the protection scheme shall be able to detect) must suit the corresponding application. So its choice depends on the protected object, the minimum fault level and/or the type of neutral point earthing. The choice is typically made by protection engineers according to their practice or e.g. as per ENA standard ([2]). Exemplarily, choosing the primary fault sensitivity for busbars, the rated load of the outgoing feeder $I_{r,load}$ or rating of the circuit breaker or minimum fault level $I''_{sc,min,int}$ can be considered.

Having chosen the primary fault sensitivity $I_{p,des}$ of the scheme, the secondary setting of the relay I_{set} can be calculated bearing in mind that the elements connected together within a high impedance protection scheme will decrease the sensitivity consuming a portion of current at the corresponding scheme setting voltage U_{set} (i.e. exciting currents I_e of the CTs, varistor spill current I_{var} at the setting voltage):

$$I_{set} = \frac{I_{p,des}}{k_r} - \sum_{x=1}^{N_{CT}} \frac{U_{set}}{E_{k,x}} I_{e.x} - I_{var}(U_{set}) \approx \frac{I_{p,des}}{k_r} - N_{CT} \frac{U_{set}}{E_k} I_e - I_{var}(U_{set}) \tag{6}$$

Remark: A rough calculation as per right side of the Eq. (6) is enough for most practical cases. Thereby, often the 'worst-case' CT data are considered, i.e. the lowest E_k, the highest I_e. This has an influence on the calculated sensitivity, so the real fault sensitivity can differ (is higher in this case). This fact shall be considered when choosing required primary fault sensitivity.

1.3.4 Calculation of the required stabilizing resistor

With the steps described in items Error! Reference source not found. and Error! Reference source not found. the basic properties of the high impedance protection scheme were calculated: the scheme setting voltage U_{set} and the current setting of the relay I_{set}.

The multifunctional relay SIPROTEC 5 7SJ8x requires external stabilizing resistor R_{stab} to be connected in series to the relay input in order to assure the necessary scheme setting voltage U_{set}.

The value of the stabilizing resistor can be calculated in straightforward way using the scheme setting voltage U_{set} and the setting of the relay I_{set}, as chosen in the previous steps:

$$R_{\text{stab}} = \frac{U_{\text{set}}}{I_{\text{set}}} - R_{\text{relay}} \approx \frac{U_{\text{set}}}{I_{\text{set}}} \tag{7}$$

Thereby, the relay input burden R_{relay} can be typically neglected.

1.3.5 Calculation of the required non-linear resistor (varistor)

As stated in the previous chapters, during an internal fault high voltage may arise across the differential branch (i.e. the tie with relay and R_{stab} connected in series). Therefore, non-linear resistors are necessary in order to avoid secondary circuits (wirings, CT clamps, resistors, etc) be exposed to high voltages. Such varistors shall be connected across the differential branch.

The secondary circuits are typically designed to withstand 3000 V peak. In practice, in order to safely protect secondary circuits of high impedance schemes the usage of a varistor is necessary when the voltage across the differential branch may exceed around 1500 V rms, which is 2121 V peak. That can be rounded down with a safety margin to 2000 V peak.

In order to estimate whether this voltage may appear in the designed scheme, at first the theoretical rms voltage $U_{\text{sc,max,int,rms}}$ which would occur across the differential branch if CT did not saturate shall be determined according to the following equation:

$$U_{\text{sc,max,int,rms}} = \frac{I''_{\text{sc,max,int}}}{k_{\text{r}}} \left(R_{\text{relay}} + R_{\text{stab}} \right) \tag{8}$$

Considering CT saturation, the resulting maximum peak voltage across the differential branch $\hat{U}_{\text{max,tie}}$ can be calculated [2]:

$$\hat{U}_{\text{max,tie}} = 2\sqrt{2E_{\text{k}}\left(U_{\text{sc,max,int,rms}} - E_{\text{k}}\right)} \tag{9}$$

Summarizing, when the relationship in (10) is fulfilled the usage of varistor is mandatory:

$$\hat{U}_{\text{max,tie}} > 2000\,\text{V} \tag{10}$$

Remark: High impedance restricted earth-fault protection applications may sometimes not require varistor, but busbar protection applications in general do. However, it is considered as good practice to equip with a varistor all high impedance protection installations.

The protection level of the varistor can be estimated from its characteristic (for dc or instantaneous values)

$$\hat{U}_{\text{var}} = C \cdot \hat{I}^{\,\beta}, \tag{11}$$

where the constants C and β shall be given by the varistor manufacturer.

The rms protection level is then: $U_{\text{var}} \sim \hat{U}_{\text{var}} / \sqrt{2}$, (12)

1.3.6 Calculation of the required thermal ratings of the auxiliary components: Stabilizing resistors and varistors

The ratings of both components, stabilizing resistor and varistor, shall be then chosen to match the application.

1.3.6.1 Thermal rating of varistor

The varistor shall be chosen to match the differential branch setting voltage and to limit the voltage to a safe value. i.e. its characteristic must not change significantly for voltages below and beyond the differential branch setting U_{set} up to the voltage limit of e.g. 2000 V peak. The varistor must be also capable of passing the maximum prospective fault current that can be transformed by the CT.

The type of varistor required can be typically chosen by calculating its necessary thermal rating as defined by the following empiric formula:

$$P_{\text{var}} = \frac{4}{\pi} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}} E_{\text{k}} \quad (13)$$

The absorbed thermal energy during internal short-circuit current flow is then

$$W_{\text{var}} = P_{\text{var}} \cdot t_{\text{sc}} \quad (14)$$

During scheme design one shall determine the maximum duration of fault t_{sc} and calculate the energy dissipation rating using Eq. (14). Since the varistor shall practically withstand the CB-fail or protection fail conditions during an internal fault, the maximum fault clearance time t_{sc} taken as of 1 s is typically sufficient. Therefore, the result of calculation according to Eq.(14) can be compared to 1 second rating of the varistor.

Regarding thermal rating of the varistor the following issues shall be considered:

a) One shall note that in high impedance schemes utilizing CTs with $E_{\text{k}} > U_{\text{var}}$ the Eq.(13) provides too large values as they may appear in the real scheme with varistor applied (since the varistor becomes low-ohmic at voltages below E_{k}, leading to the fact that CTs do not saturate, so the amount of energy delivered to the scheme is then limited not by the knee-point emf but by the varistor protection voltage U_{var}). In such cases it is proposed to estimate the thermal rating according to the empiric formula (15):

$$P_{\text{var,mod}} = \frac{4}{\pi} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}} U_{\text{var}} \quad (15)$$

, for $E_{\text{k}} > U_{\text{var}}$

b) Furthermore, the calculation of thermal rating of the varistor does not include the energy absorption by the stabilizing resistor during an internal fault.

c) However, in case when varistor will be taken out of operation (damaged, etc.), the energy as per Eq.(13) will appear and dissipate on the stabilizing resistor alone. This issue can be considered by choosing (limiting) knee point emfs of the CTs.

d) the calculation as per Eq.(13) can be seen as being on the safe side, as long as the real (measured) E_{k} of the CT is known. Care shall be taken to cases when nameplate data of E_{k} is used. As per IEC

tandard [1] the E_k on the nameplate is the minimum value, which can be (even considerably) smaller than the real (measured) knee-point emf.

In addition to the thermal rating of the varistor the following recommendation shall be fulfilled:

1. At setting voltage of the scheme U_{set} the varistor rms current I_{var}, calculated as per Eq.(16) shall not exceed 30mA in high impedance schemes utilizing CTs with 1 A secondary rated current, and 100mA in high impedance schemes utilizing CTs with 5 A rated current (not recommended).

$$I_{var} = 0.52 \cdot \left(\sqrt{2} \cdot \frac{U_{set}}{C} \right)^{1/\beta} \quad (16)$$

Summarizing the above, in most cases this practically leads to a choice between two main types of varistor available from e.g. Metrosil for high impedance schemes utilizing CTs with 1 A secondary rated current, as shown in Table 1.

Table 1 Proposed Metrosil varistor types for high impedance circuits with 1 A secondary (mostly used)

Metrosil identification (type)	Parameters of the varistor characteristic			Recom. max branch setting voltage U_{set} [Vrms]	Rated energy absorp. for 200°C temp rise W_{var} [J]	Short Time Current [Arms]		
	C	□	□			1s	2s	3s
600A/S1/S256 (single pole) 600A/S3/1/802 (three pole)	450	0.25	0.87	125	53333	45	30	22
600A/S1/S1088 (single pole) 600A/S3/1/S1195 (three pole)	900	0.25	0.87	300	88000	39	23	17

Remark: Also different types / different manufacturers of varistors can be used in high impedance protection applications.

Remark: In high impedance schemes utilizing CTs with 5 A rating (not recommended) different types of varistors may apply.

1.3.6.2 Thermal rating of stabilizing resistor

The thermal rating of the stabilizing resistor is typically carried out considering the following steps:

At first, the continuous power rating of the stabilizing resistor can be chosen as per (17):

$$P_{stab,cont} \geq \frac{U_{set}^2}{R_{stab}} \quad (17)$$

Remark: It shall be noted that in order to keep the resistor healthy during commissioning tests the fault current from the testing equipment should be immediately withdrawn after the device gives a protection trip.

In second step, R_{stab} must have a short time rating large enough to withstand the fault current before the fault is cleared. Thereby, the rms voltage developed across the stabilizing resistor during maximal prospective internal fault $U_{rms,f}$ is decisive for the thermal stress of the stabilizing resistor. (18)

It is calculated according to mathematically derived formula:

$$U_{rms,f} = 1.3 \cdot \sqrt[4]{E_k^3 \cdot R_{stab} \cdot \frac{I_{sc,max,int}}{k_r}}$$

The time duration of 0.5 seconds can be typically considered for the stabilizing resistor ($P_{stab,0.5s}$).

Remark: Longer times as e.g. 1 s may lead to very huge resistors. The consideration of longer times is impracticable, especially taking into consideration that within the scheme also a varistor is applied, which takes over a part of the thermal energy. The considerations presented here are not taking the varistor into account. Therefore, the 0.5 s rating is on a safe side.

Summarizing, the resulting short-time rating $P_{stab,0.5s}$ shall be then chosen as per Eq. (19):

$$P_{stab,0.5s} \geq \frac{U_{rms,f}{}^2}{R_{stab}} \tag{19}$$

Regarding thermal rating of the stabilizing resistor the following issues shall be considered:

a) One shall note that in high impedance schemes utilizing CTs with $E_k > U_{var}$ the Eq. (19) provides too large values as they may appear in the real scheme with varistor applied (since the varistor becomes low-ohmic at voltages below E_k, leading to the fact that CTs do not saturate, so the amount of energy delivered to the scheme is then limited not by the knee-point emf but by the varistor protection voltage U_{var}). In such cases it is proposed to estimate the thermal rating exchanging $U_{rms,f}$ in Eq.(19) by $U_{rms,f,mod}$ calculated according to the empirically verified formula (20):

$$U_{rms,f,mod} = 1.3 \cdot \sqrt[4]{U_{var}{}^3 \cdot R_{stab} \cdot \frac{I_{sc,max,int}}{k_r}} \quad \text{, for } E_k > U_{var} \tag{20}$$

b) Furthermore, the calculation of thermal rating of the stabilizing resistor does not include the considerable energy absorption by the varistor resistor during an internal fault.

c) The distribution of the dissipated energy during an internal fault between the stabilizing resistor and varistor is not linear and depends on varistor protection voltage U_{var} and CTs knee-point emf E_k together with stability (setting) voltage of the scheme U_{set}. Simplifying, the higher the ratio U_{var} / U_{set} the more energy will be dissipated on the resistor.

d) However, in case when varistor will be taken out of operation (damaged, etc.), the energy as per Eq. (13) will appear and dissipate on the stabilizing resistor alone. This issue can be considered by choosing (limiting) knee point emfs of the CTs.

e) the calculation as per Eq.(19) and respective Eq. (18) can be seen as being on the safe side, as long as the real (measured) E_k of the CT is known. Care shall be taken to cases when nameplate data of E_k is used. As per IEC standard [1] the E_k on the nameplate is the minimum value, which can be (even considerably) smaller than the real (measured) knee-point emf.

1.3.7 Final check of the scheme sensitivity

In the final stage the final scheme sensitivity can be chosen by applying the Eq. (21) with known varistor spill current, as per Eq.(16).

$$I_{p,des,final} = k_r \cdot I_{set} + k_r \cdot \left(\sum_{x=1}^{N_{CT}} \frac{U_{set}}{E_{k,x}} I_{e,x} + I_{var}(U_{set}) \right) \approx k_r \cdot \left[I_{set} + N_{CT} \frac{U_{set}}{E_k} I_e + I_{var}(U_{set}) \right] \tag{21}$$

1.4 Working example

This chapter provides working example showing relevant calculations for a chosen application. Exemplarily, a busbar protection application is taken.

1.4.1 Relevant required data

1.4.1.1 Power system data

The relevant power system primary data in case of busbar protection in transmission systems are taken as follows:

- the maximum symmetrical short-circuit current for external (through) faults $I''_{sc,max,ext} = 63\text{kA}$
- the maximum symmetrical short-circuit current for internal faults $I''_{sc,max,int} = 63\,\text{kA}$

In case of a busbar, for both above quantities the maximum short-time symmetrical short-circuit withstand current of the switchgear $I''_{sc,max,swg}$ is considered. :

- the rating of the circuit breakers / busbar rating equals to $I_{r,load} = 4000\,\text{A}$
- the minimum symmetrical short-circuit current for internal faults is assumed at $I''_{sc,min,int} = 15\text{kA}$ for phase-to-phase-fault current (as in typical solidly earthed transmission system the single-pole fault current at the busbar is slightly higher or slightly lower than the three-pole)

1.4.1.2 Current transformer data

The CTs used in the high impedance scheme are of equal ratios, low leakage type of IEC class PX.

- the number of CT that belong to the considered /designed differential protection zone $N_{CT} = 8$

IEC class PX [1] parameters are as follows :

- CT ratio: 4000A/1A; i.e. $k_r = \frac{I_{pr}}{I_{sr}} = \frac{4000\,\text{A}}{1\,\text{A}} = 4000$
- CT knee-point emf $E_k = 1000\,\text{V}$
- CT exciting current at the knee-point emf $I_e = 25\,\text{mA}$
- CT secondary winding resistance $R_{CT} = 5\,\Omega$

Furthermore:

- the CT secondary wiring resistance from the CT clamps to the paralleling point of the scheme (loop resistance) equals to $R_{wire} = 0.55\,\Omega$ (corresponds to approx. 100 m loop length of copper wire with 4 mm^2 cross-section, resistance value is corrected to 75 ^{O}C e.g. for worst case calculation)

1.4.1.3 Relay data and necessary auxiliary component elements

The multifunctional relay SIPROTEC 5 7SJ8x will be used for phase-selective high impedance busbar protection application. Thereby three standard inputs A1..A6 will be used:

- operating current setting range $I_{\text{set,range}} = 0.03\text{ A}...0.001..100\text{ A}$,
- relay input burden, expressed as resistance $R_{\text{relay}} = 0.1\,\Omega$.
- the data of the system components (resistor and varistor) will be calculated in further steps

1.4.2 Calculation of the minimum required stabilizing voltage

As per Eq (1) the minimum required stability voltage of the high impedance scheme U_{stab} can be calculated, taking the given maximum through fault current $I''_{\text{sc,max,ext}} = 63\text{kA}$:

$$U_{\text{stab}} = \frac{I_{\text{max,ext}}}{k_{\text{r}}}\left(R_{\text{CT}} + R_{\text{wire}}\right) = \frac{63\text{kA}}{4000}(5 + 0.55) = 87.41\text{ V} \tag{22}$$

The setting voltage U_{set} of the scheme over the differential branch shall be made equal or greater than the required stability voltage, as calculated in Eq.(22). Let's take:

$$U_{\text{set}} = 120\text{ V} \tag{23}$$

1.4.3 Calculation of the required fault setting

To assure the functionality of the scheme (trip on internal fault), the CT knee-point emf E_{k} shall fulfill the requirement as given in Eq (3):

$$E_{\text{k}} \geq 2 \cdot U_{\text{set}}\text{ , i.e.: } 1000\text{ V} \geq 2 \cdot 120\text{ V} = 240\text{ V} \Rightarrow \text{fulfilled} \tag{24}$$

In order to reach the desired scheme sensitivity, i.e. to trip on internal fault, the current setting of the relay in the differential branch shall be now calculated.

Considering that the minimum fault current at the busbar is quite high, the desired primary fault sensitivity $I_{\text{p,des}}$ is chosen (exemplarily for this working example) at 50 % of the rating of the busbar:.

$$I_{\text{p,des}} = 2000\,\text{A} \tag{25}$$

Remark: Please note that the primary fault sensitivity for busbar can be chosen at different level. This depends on customer philosophy and experience.

Having chosen the primary fault sensitivity $I_{\text{p,des}}$ of the scheme, the secondary setting of the relay I_{set} can be calculated as per Eq. (6). The varistor spill current will be at this stage neglected:

$$I_{\text{set}} \approx \frac{I_{\text{p,des}}}{k_{\text{r}}} - N_{\text{CT}}\frac{U_{\text{set}}}{E_{\text{k}}}I_{\text{e}} - I_{\text{var}}(U_{\text{set}}) = \frac{2000\text{ A}}{4000} - 8\frac{120\text{ V}}{1000\text{ V}}0.025\text{ A} = 0.476\text{ A} \tag{26}$$

The setting current I_{set} of the scheme will be then taken:

$$I_{\text{set}} = 0.5\text{ A} \tag{27}$$

1.4.4 Calculation of the required stabilizing resistor

With the scheme setting voltage U_{set} and the current setting of the relay I_{set} . the resistance value of the external stabilizing resistor R_{stab} can be calculated as per Eq.(7):

$$R_{stab} = \frac{U_{set}}{I_{set}} - R_{relay} \approx \frac{U_{set}}{I_{set}} = \frac{120\,V}{0.5\,A} = 240\,\Omega \quad (28)$$

Thereby, the relay input burden R_{relay} was neglected.

The thermal rating of the resistor is calculated:

The continuous power rating of the stabilizing resistor can be chosen as per Eq. (17):

$$P_{stab,cont} \geq \frac{U_{set}^{\ 2}}{R_{stab}} = \frac{120^2\ V^2}{240\ \Omega} = 60\ W \quad (29)$$

Remark: It shall be noted that in order to keep the resistor healthy during commissioning tests the fault current from the testing equipment should be immediately withdrawn after the device gives a protection trip.

Furthermore, R_{stab} must have a short time rating large enough to withstand the fault current before the fault is cleared. Thereby, the rms voltage developed across the stabilizing resistor during maximal prospective internal fault $U_{rms,f}$ is decisive for the thermal stress of the stabilizing resistor. It is calculated according to Eq.(18):

$$U_{rms,f} = 1.3 \cdot \sqrt[4]{E_k^{\ 3} \cdot R_{stab} \cdot \frac{I_{sc,max,int}}{k_r}} = 1.3 \cdot \sqrt[4]{(1000\,V)^3 \cdot 240\,\Omega \cdot \frac{63000\,A}{4000}} = 1812.7\,V \quad (30)$$

The time duration of 0.5 seconds can be typically considered for the stabilizing resistor ($P_{stab,0.5s}$).

The resulting short-time rating $P_{stab,0.5s}$ shall be then chosen as per Eq.(19) :

$$P_{stab,0.5s} \geq \frac{U_{rms,f}^{\ 2}}{R_{stab}} = \frac{(1812.7\,V)^2}{240\,\Omega} = 13691\ W \quad (31)$$

Therefore:

Resistor chosen (per relay input): $R_{stab} = 240\,\Omega$, $P_{stab,cont} \geq 60W$, $P_{stab,0.5s} \geq 13691\ W$ (32)

Regarding short-time thermal rating remarks in chapter Error! Reference source not found. shall be considered in case when size of resistor shall be too large for the given protection cubicle.

1.4.5 Calculation for the required non-linear resistor (varistor)

During an internal fault high voltage may arise across the differential branch (i.e. the tie with relay and R_{stab} connected in series). Therefore, non-linear resistors are necessary in order to avoid secondary circuits (wirings, CT clamps, resistors, etc) be exposed to high voltages. Such varistors shall be connected across the differential branch.

In order to estimate this voltage which may appear in the designed scheme, at first the theoretical rms voltage $U_{sc,max,int,rms}$ which would occur across the differential branch if CT did not saturate is determined according to Eq.(8):

$$U_{sc,max,int,rms} = \frac{I''_{sc,max,int}}{k_r}\left(R_{relay} + R_{stab}\right) = \frac{63\,kA}{4000}(0.05\,\Omega + 240\,\Omega) = 3780\,V \quad (33)$$

Considering CT saturation, the resulting maximum peak voltage across the differential branch $\hat{U}_{\text{max,tie}}$ is calculated:

$$\hat{U}_{\text{max,tie}} = 2\sqrt{2E_{\text{k}}\left(U_{\text{sc,max,int,rms}} - E_{\text{k}}\right)} = 2\sqrt{2000\,\text{V}\left(3780\,\text{V} - 1000\,\text{V}\right)} = 4716\,\text{V} \tag{34}$$

When the relationship in (10) is fulfilled the usage of varistor is mandatory:

$$\hat{U}_{\text{max,tie}} > 2000\text{V} \Leftrightarrow 4716\text{V} > 2000\text{V} \Rightarrow \text{varistornecessary} \tag{35}$$

Considering scheme setting voltage U_{set} of 120 V (very close to the recommended limit of 125 V for the smaller varistor) a Varisor of type 600A/S3/1/S1195 (three pole) or three varistor of type 600A/S1/S1088 can be chosen (see Table 1).

The protection level of this varistor can be estimated from its characteristic (for dc or instantaneous values) where the constants C and β are given in Table 1 and the maximum prospective secondary current for the internal fault:

$$\hat{U}_{\text{var}} = C \cdot \hat{I}^{\ \beta} = 900 \cdot \left(\sqrt{2} \cdot \frac{63000}{4000}\right)^{0.25} = 1955\ \text{V}\,, \tag{36}$$

The rms protection level is then:

$$U_{\text{var}} \sim \hat{U}_{\text{var}} / \sqrt{2} = 1383\text{V}\,, \tag{37}$$

Its rms spill current at the setting voltage of the scheme (Eq.(16):

$$I_{\text{var}} = 0.52 \cdot \left(\sqrt{2} \cdot \frac{U_{\text{set}}}{C}\right)^{1/\beta} = 0.66\,\text{mA} \tag{38}$$

The requirement that at the setting voltage the spill current shall be less than 30 mA (CTs with 1 A secondary) is then fulfilled.
The necessary thermal rating of the varistor can be calculated using Eq.(13)

$$P_{\text{var}} = \frac{4}{\pi} \cdot \frac{I_{\text{sc,max,int}}}{k_{\text{r}}} E_{\text{k}} = \frac{4}{\pi} \cdot \frac{63000\,\text{A}}{4000} 1000\,\text{V} = 20053.5\,\text{J/s} \tag{39}$$

This necessary thermal rating is smaller than the maximum thermal rating of 88000 J (see Table 1).This maximum energy rating will not be even exceeded by the short-circuit flow of 4 s.
Therefore:

Varistor chosen: one of 600A/S3/1/S1195 (three pole) type
or three varistors of type 600A/S1/S1088 (40)

1.4.6 Final check of the scheme sensitivity

In the final stage the final scheme sensitivity can be chosen by applying the Eq. (21) with known varistor spill current, as per calculation in Eq.(38):

$$\begin{aligned} I_{\text{p,des,final}} &\approx k_{\text{r}} \cdot \left[I_{\text{set}} + N_{\text{CT}} \frac{U_{\text{set}}}{E_{\text{k}}} I_{\text{e}} + I_{\text{var}}(U_{\text{set}}) \right] = \\ &= 4000 \cdot \left[0.5\,\text{A} + 8\frac{120\,\text{V}}{1000\,\text{V}} 0.025\,\text{A} + 0.00066\,\text{A}) \right] = 4000 \cdot 0.52466\,\text{A} = 2098.6\,\text{A} \end{aligned} \tag{41}$$

This corresponds to 52.4 % of the rating of the busbar (4000 A) and fulfills the requested fault setting for this example.

1.4.7 Scheme settings

The following is then set in SIPROTEC 5 7SJ8x for the main function (high impedance protection trip):

VI 3ph 1; 50/51 OC-3ph-B1, Definite–T 1

821.1941.661.1	Mode	on	
_._.661.2	Operate & flt. rec. blocked	no	
_._.661.8	Method of measurement	fundamental comp.	
_._.661.3	Threshold (fault setting I_{set})	0.5A	Range: 0.03A ...100A, stps. 0.001A
_._.661.6	Operate delay	0.0 s	Range: 0s ...60s, stps. 0.01s

Furthermore the following high impedance scheme components are necessary:

Resistor chosen (pro relay input):	$R_{stab} = 240\,\Omega$, $P_{stab,cont} \geq = 60\,W$, $P_{stab,0.5s} \geq 13691$ W

Varistor chosen:	one of 600A/S3/1/S1195 (three pole) type or three varistors of type 600A/S1/S1088

1.4.7.1 CT supervision

The CT circuit supervision can be incorporated within the relay, as well. It can be realized using e.g. Definite–T 2 stage of the multifunctional relay SIPROTEC 5 7SJ8x:
Depending on the loading conditions, the CT supervision can be set to detect approx. 12 % of the full loading of the busbar, i.e. 0,12 · 4000 A = 480 A primary. The secondary setting that can be incorporated will be then 0.1 A (24 V setting of the scheme) correspondingly. This leads to the final supervision sensitivity as per Eq (42):

$$I_{superv} \approx k_r \cdot \left[I_{set} + N_{CT} \frac{U_{set}}{E_k} I_e + I_{var}(U_{set}) \right] = \\ = 4000 \cdot \left[0.1\,A + 8 \frac{120\,V}{1000\,V} 0.025\,A + 0.00066\,A) \right] = 4000 \cdot 0.12466\,A = 498.6\,A \quad (42)$$

This corresponds to 12.5 % of the rating of the busbar (4000 A) and fulfills the requested CT supervision setting for this example.

The corresponding settings for e.g. Definite–T 2 stage in SIPROTEC 5 7SJ8x will be:
VI 3ph 1; 50/51 OC-3ph-B1, Definite–T 2

821.1941.662.1	Mode	on	
_._.662.2	Operate & flt. rec. blocked	no	
_._.662.8	Method of measurement	fundamental comp.	
_._.662.3	Threshold (superv. setting I_{superv}) alarm only	0.1A	Range: 0.03A ...100A, stps. 0.001A

_._.662.6	Operate delay	oo s Range: 0s ...60s, stps. 0.01s

It is important to configure the Definite T – 2 stage for issuing alarm only.
In general, there are several options for further use of the CT supervision alarm. In this worked example this alarm signal will be available after 5 sec based on the timer setting Operate Time Delay. The following options can be chosen:
1. Sending the alarm only (via binary output or via communication protocol).
2. Additionally to 1, route the alarm signal within the relay in order to block the Trip , Definite – T1 element
This will avoid a trip of the high impedance busbar protection in case of a through fault under CT broken wire conditions. Please note that this measure will not protect the CT inputs of the relay and the stabilizing resistor / varistor against damage under longer lasting through fault conditions.
3. Additionally to 1 and 2, energize an external CT shorting relay with one coil and at least four related contacts (e.g. 7PA23). The lock-out relay has to be energized by the CT supervision alarm signal. One contact should be placed in front of the varistor to short circuit each CT input of SIPROTEC 5 7SJ8x. The fourth contact of the relay can be used for signaling the 'high impedance busbar out-of-service' information. The reset of the external lock-out relay has to be done manually.

This measure will protect the CT inputs of the relay and the stabilizing resistor against damage under longer lasting through fault conditions.
Alternatively (depending on customer practice), a separate CT supervision relay may be used.
The types of further auxiliary components like CT shortening relay, CB lock-out and test switches can be chosen as per respective customer practice.

1.4.8 Connection example

A connection example for the working example is shown in Figure 2. Trip relay is of Fast type (Type F) or alternatively, a High-Speed relay with Semiconductor Acceleration (type HS) can be used. The CT supervision is realized within the relay in this connection example (using Definite T – 2 stage).

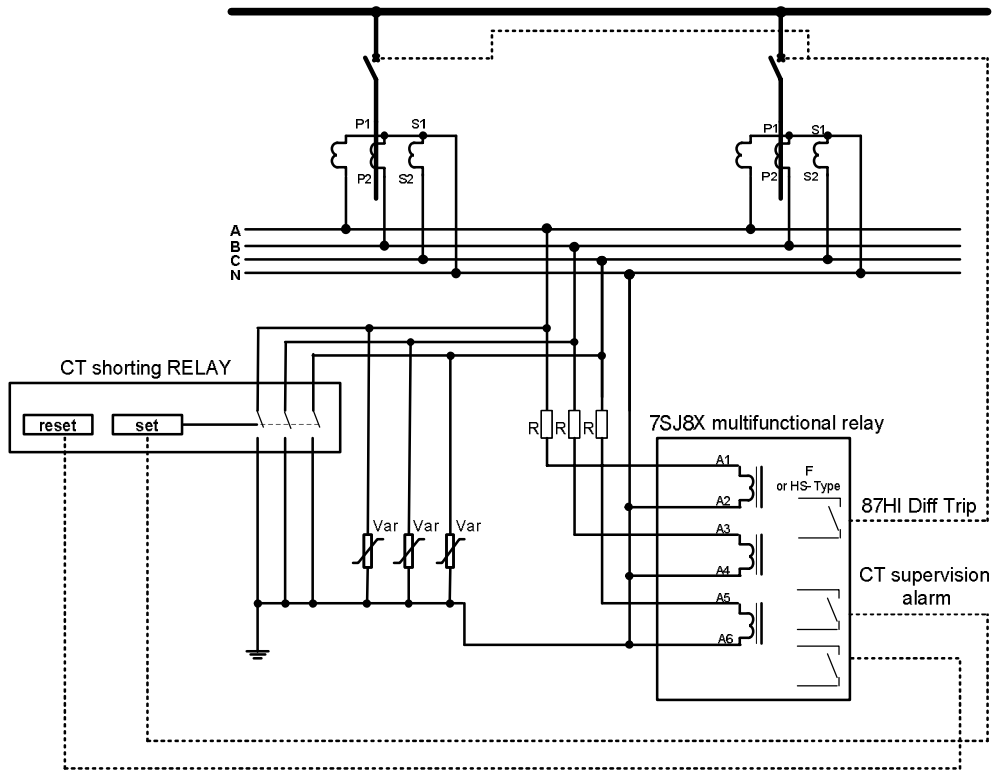


Figure 2 Connection of the high impedance scheme for the working example

1.5 Applications

As already mentioned in chapter Error! Reference source not found. the multifunctional relay SIPROTEC 5 7SJ8x can be used within all the mentioned high impedance protection schemes, both for phase-segregated circulating current high impedance protection applications, as well as for single phase restricted earth fault protection applications.

For the sake of completeness scheme setting hints for some major applications are shown in following.

1.5.1 Phase and earth-fault high impedance differential protection of busbars

The scheme stability setting (voltage over differential branch) [2]:

- maximum symmetrical short-circuit withstand current of the switchgear

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below:

- 10.. 30 % of minimum fault current available as per standard [2] , or as may be agreed
- %. of busbar rating (e.g. 33 % or 50 %)
- % of outgoing feeder rating (e.g. 100 % or 120 %)

Remark: High impedance protection scheme is widely used for busbar arrangements like single busbars, single busbars with sectionalizers, or circuit-breaker-and-a-half arrangements. The usage of high impedance busbar protection for double- and more sections busbars (with isolators) is not recommended, because of high complexity related to switching-over of CT secondaries that decreases the scheme reliability.

The high impedance protection scheme for busbar is shown exemplarily in Figure 3

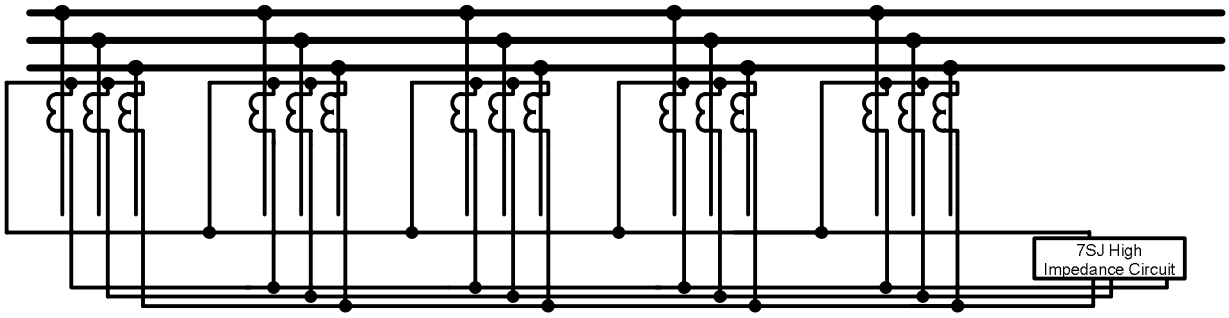


Figure 3 Phase and earth-fault high impedance differential protection of busbars

1.5.2 Phase and earth-fault high impedance differential protection of auto transformers

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) at the LV side of the transformer, the latter can be taken as of 16 times the rated current of the LV side of the transformer (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- for transformer winding solidly connected to earth: 10.. 60 % of the rated current of the HV winding
- for transformers winding earthed via impedance 10.. 25 % of minimum fault current available for an earth-fault at transformer terminals

The high impedance protection scheme for auto-transformers is shown exemplarily in Figure 4

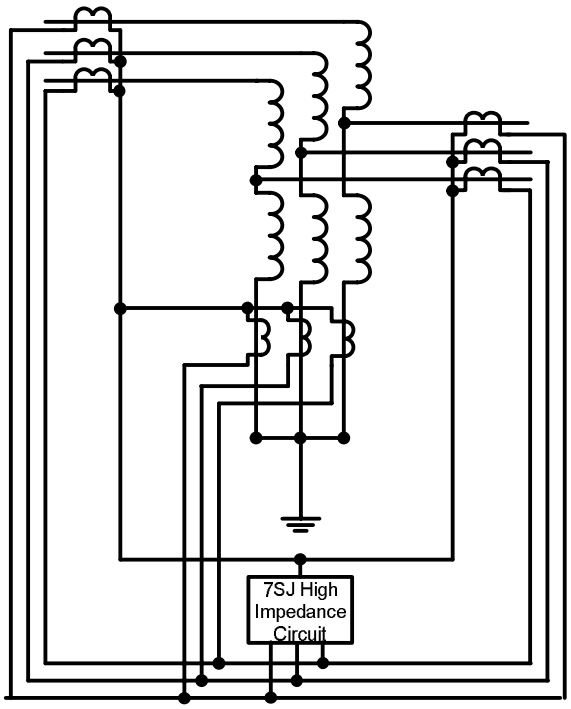


Figure 4 Phase and earth-fault high impedance differential protection of auto-transformers

1.5.3 Phase and earth-fault high impedance differential protection of motors or generators (synchronous)

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the synchronous machines, the latter can be taken as of 12.5 times the rated current of the series reactor winding (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- less than 10 % of the rated current of the protected winding of the synchronous machine

1.5.4 Phase and earth-fault high impedance differential protection of series reactors

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the series reactor, the latter can be taken as of 20 times the rated current of the series reactor winding (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- 10.. 30 % of minimum fault current available for a-fault at series reactor terminals

1.5.5 Phase and earth-fault high impedance differential protection of shunt reactors

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the shunt reactor, the latter can be taken as of 10 times the rated current of the shunt reactor winding (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- 10.. 25 % of minimum fault current available for a-fault at shunt reactor terminals

In Figure 5 high impedance scheme of series reactors, shunt reactors, motors or generators is shown

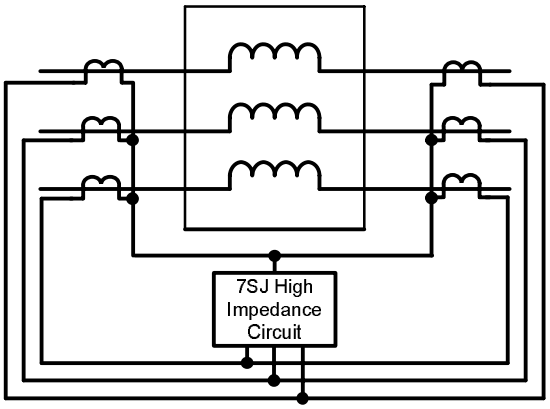


Figure 5 Phase and earth-fault high impedance differential protection of series reactors, shunt reactors, motors or generators

1.5.6 Restricted earth fault (REF) protection schemes of transformer windings

The scheme stability setting (voltage over differential branch):

- maximum symmetrical short-circuit current for external faults (through-faults) of the protected transformer winding, the latter can be taken as of 16 times the rated current of the protected winding of the transformer (or other value as may be agreed) as per [2]

The scheme sensitivity setting (fault setting or primary operating current), can be chosen as one of the shown below [2]:

- for transformer winding solidly connected to earth: 10.. 60 % of the rated current of the winding
- for transformers winding earthed via impedance or isolated: 10.. 25 % of minimum fault current available for an earth-fault at transformer terminals

The high impedance protection scheme for transformer windings is shown exemplarily in Figure 6.

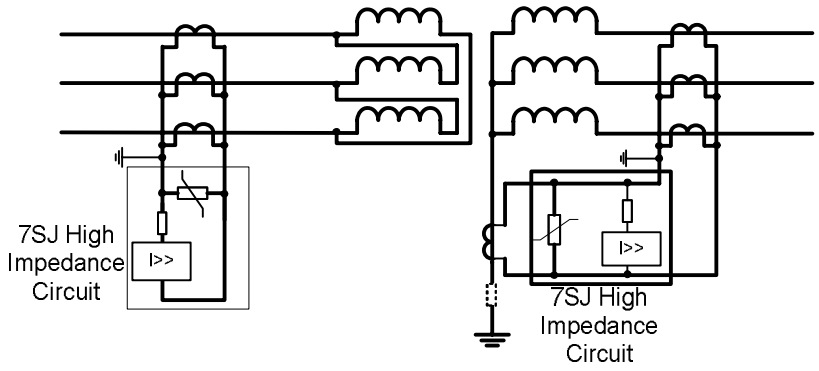


Figure 6 Restricted earth-fault high impedance differential protection of transformers

1.6 Testing procedure and test results for 87B HI

1.6.1 Simulation environment set-up

The high impedance circuit behaviour simulations were carried out within tailored simulation environment using our experience with transient CT behaviour (www.siemens.com/ctdim). Thereby, the following primary circuit configuration was considered:

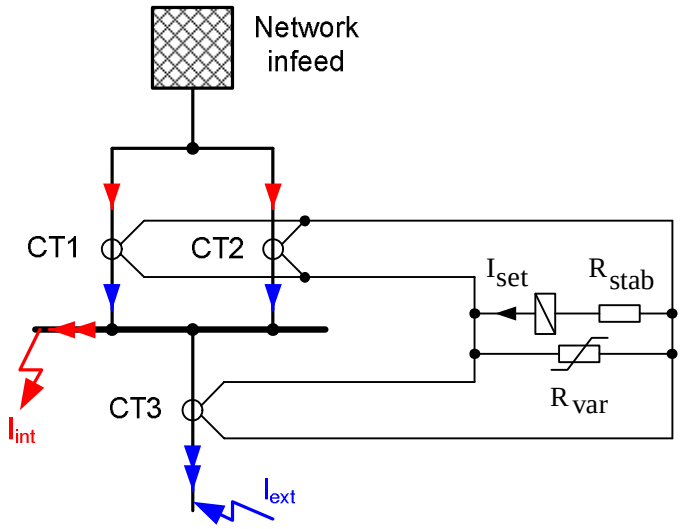


Figure 7 Scheme used for high impedance busbar circuit simulations (simplified, showing single-phase only)

The detailed secondary circuit of the current transformers can be seen in Figure 8 correspondingly.

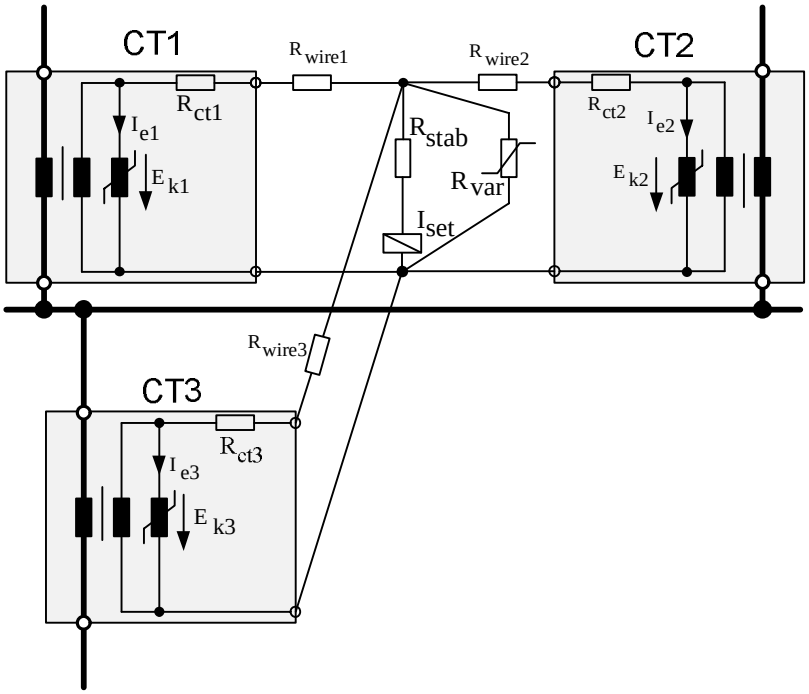


Figure 8 Scheme used for high impedance busbar circuit simulations (showing secondary circuit, single-phase only) .

1.6.2 Summarized simulation parameters 87B HI

The test cases were then generated by varying the CT parameters, so that behaviour of the scheme can be observed in dependency of the CT parameters within the scheme (e.g. in terms of E_k / U_{set}). Moreover, primary fault current magnitude and the respective fault inception times were varied, so that both short circuit currents with superimposed decaying DC component and without DC component were included within the tests. The duration of simulated cases was set to 1s[2].

The further parameters of the scheme were kept same during the tests to reach comparability of the results.

Below, the summarized data are presented in concise form:

General system/ protected object data:	
Protected object:	busbar
Frequency	60 Hz / 50 Hz
Rated voltage primary system	380 kV
Primary network time-constant resp. X/R of the primary system:	105 ms 40 (60Hz), 33 (50Hz)
Rated steady state symmetrical short-circuit current I_k"of the busbar (max. internal fault):	63 kA
Relevant data of the protected object: Maximum through fault current for stability of the scheme (primary value)	$I_{rfeeder}$ = 3000A 63kA

[2] This time was set so long to easy the readings of the energy dissipation on auxiliary elements in simulated cases.

Fault setting for the sensitivity of the scheme (primary value)	exemplarily taken as ~25% of the $I_{rfeeder}$ ~ striven as range between 650-750A primary
Adopted relay setting to reach the fault sensitivity (secondary value)	set to 0.2A
CT / protection scheme data:	
Number of CTs connected in parallel	3 (as shown in Figure 7)
Type:	IEC Class PX
CT Ratio:	3000 / 1 A
CT Knee point emf E_K:	varied (as multiple of U_{set})
CT Magnetizing current I_e at knee point emf:	40 mA
CT Internal burden R_{CT} at 75^0C:	7.5 Ω
Length /cross section of the secondary lead from the CT to the paralleling point e.g. within protection cubicle:	150 m /4mm^2 ~1.6 Ω
Stabilizing resistor used:	$R_{stab} = 1200\ \Omega$
Non-linear resistor MOV:	Metrosil 600A/S1/Spec.1088
Simulation framework:	
Fault duration simulated:	1 s
Fault inception angle:	varied 0°, 90° referred to the voltage L1
Short circuit current value	simulated as internal with variable range (as multiple of $I_{p,des}$) and external
Hardware configuration:	
Product code (MLFB)	7SJ85-????-???-??????-?Z01?2-23??2A-EBA000-000AA0-CB2BA1-CE0
Serial number	BMTTTT123456_BF1108112355
Configuration version	V05.00.05
Communication configuration version	V05.00.00
OMICRON Test Universe Version:	V.2.41 SP2013-06

Summarizing, a typical high impedance busbar protection scheme of setting voltage U_{set} of 240 V, R_{stab} of 1200 Ω, and the relay setting I_{set} of 0.2 A[3] was used. Those parameters were kept same in the simulated cases to reach comparability of the test results. The resulting primary fault sensitivity was then around 700A primary[4]. For each case the current transformer sizing reports were carried out using software tool CTDim. An exemplary report is presented in item Error! Reference source not found..

The tests were carried out using OMICRON Test Universe - Advanced TransPlay, The testing stand is shown in Figure 9.

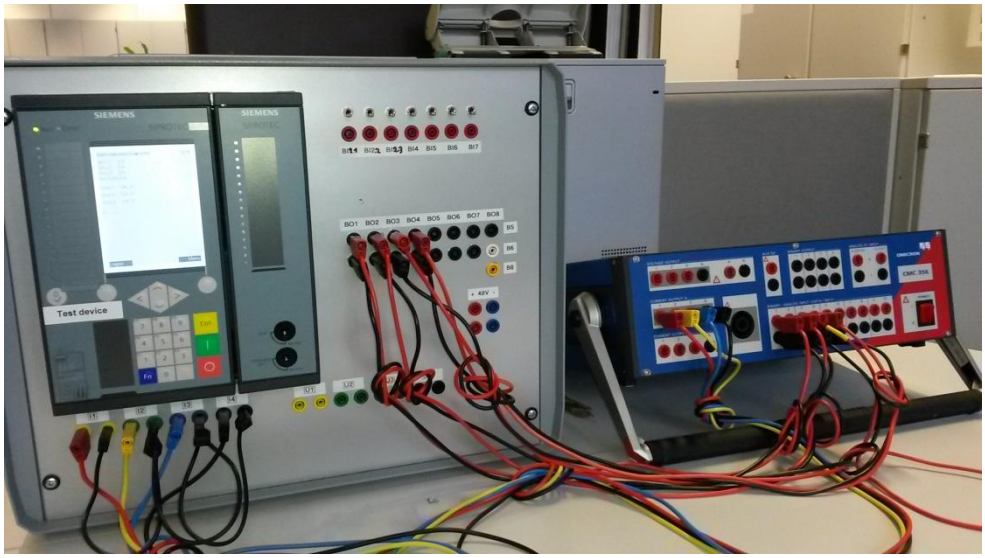


Figure 9 Equipment used during tests

1.6.2.1 Protection device settings used within 87B HI tests

The testing procedure includes observation of the behaviour of the overcurrent stages available within SIPROTEC 5 7SJ8X relay. The goal is to find out which measurement method (i.e. based on fundamental component, true rms or instantaneous values) is optimal for the usage in high impedance protection schemes.

Therefore, the function Overcurrent protection, phases – basic (50/51 OC-3ph-B) was chosen. Within this function the stage Definite–T 1 was parameterized to operate with fundamental component measurement method, and a further stage Definite–T 2 was parameterized to operate with (true) rms component measurement method.

Additionally, as a third element the function Instantaneous high-current tripping was chosen and the stage Standard 1 was activated that uses instantaneous value measurement.

Summarizing, for one test shot, all the three stages were activated as shown in Figure 10 and their reaction was observed. Moreover, considering chosen fault setting for the tests (see previous chapter), the following was set to the tested relay SIPROTEC 5 7SJ85:

[3] The fault setting was chosen at a low value (some practical busbar systems may have higher setting) in order to keep the resulting differential current at lower value (so that no hardware problems with amplifying the current appear). The results are scalable also to other schemes with higher setting.

[4] The resulting final fault sensitivity depends on the actual CT parameter, as well. Since they were varied through the tested cases, the exact primary sensitivity was slightly different in each simulated case.

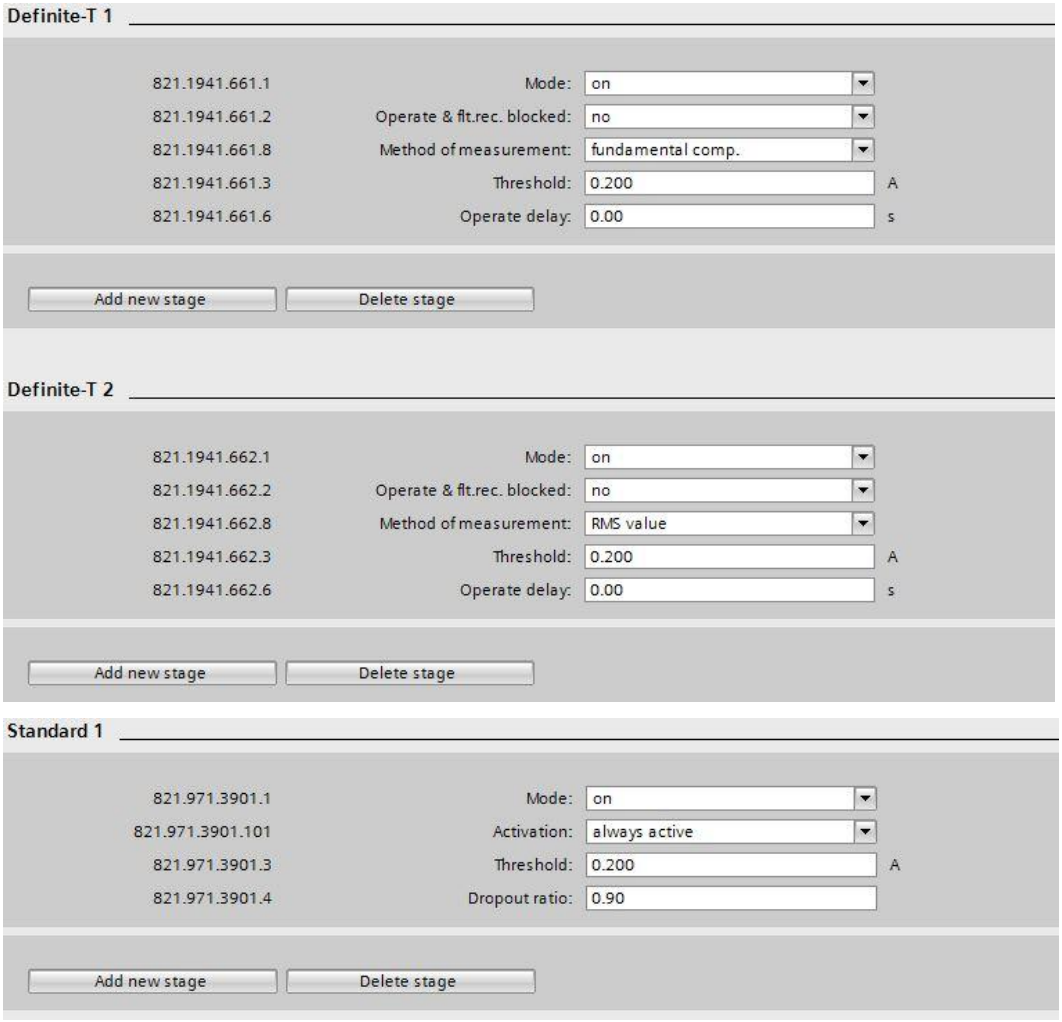


Figure 10 Settings of the 7SJ85 relay used for 87B HI tests

The tests were carried out using systems with both 60Hz and 50Hz rated frequency:

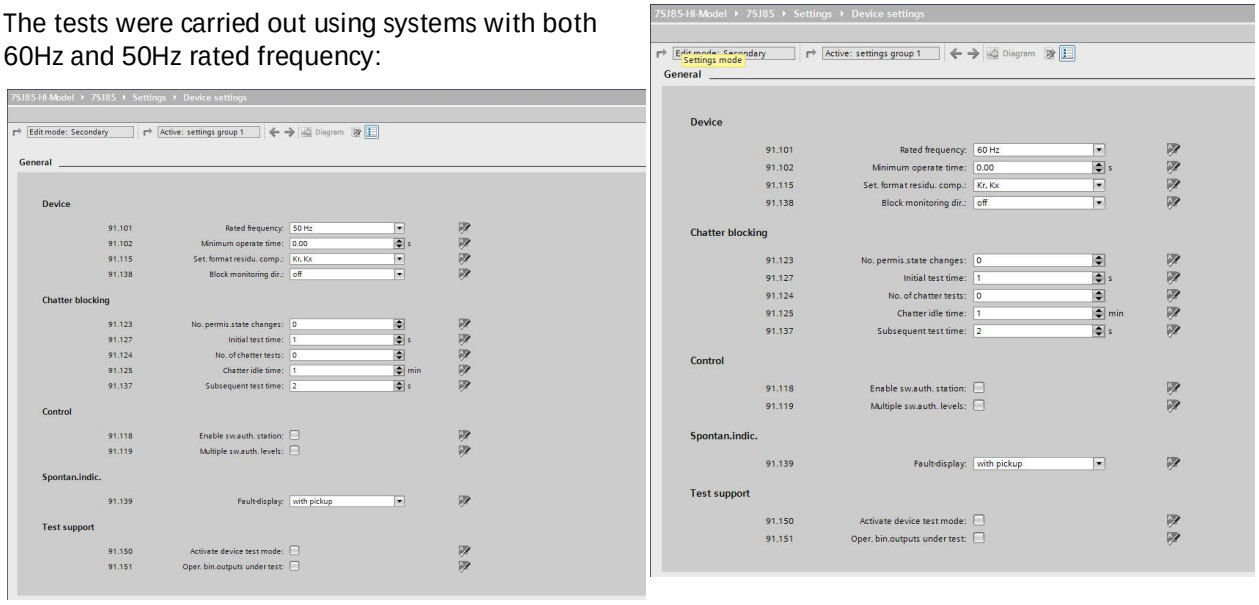


Figure 11 Device general settings for tests with 60Hz and 50 Hz

1.6.2.2 Exemplary dimensioning report (CTDim)

CT- DIMENSIONING FOR PROTECTION RELAY SIPROTEC 5 7SJ8X (87B HI)

GENERAL PROJECT DATA:

Customer:	SEC
Project:	SIPROTEC 5 7SJ8x Application Guide for 87B HI
Station:	CASE 06
Feeder:	CASE6 FLT-SENS 660A Sett.0.2A Rstab1200 Ohm Ustab240V
Issued by:	Dr. A. Bachry
Our reference:	it 200 071
Date:	12.12.2014
Remark:	fault sensitivity used: 660A

GENERAL SYSTEM AND SUBSTATION DATA:

Nominal voltage:	380 kV
Nominal frequency:	60 Hz
Rated short-circuit current of station:	63 kA
Remark:	Uk/Uset=6

DATA OF CT 1 ACCORDING TO IEC-PX:

CT type:	IEC Class PX
Transformation ratio:	3000 A / 1 A
Kneepoint voltage U_{knee}:	1440 V
Mag. current I_{knee} at U_{knee}:	0.04 A
Internal resistance R_{ct}:	7.5 Ω

RELAY DATA:

Manufacturer:	SIEMENS
Type:	SIPROTEC 5 7SJ8 (87B HI)
Internal burden:	0.1 VA
Number of CTs in parallel with relay (N)	3

CT REQUIREMENTS FOR SIPROTEC 5 7SJ8x (87B HI):

All CTs must have the same transformation ratio. To prevent maloperation of the relay during saturation of the CTs on an external fault, the actual stability voltage U_S must be at least the voltage $U_{S,min}$ produced by the maximum secondary through fault current, flowing through the cable resistance and the CTs' internal resistance:

$$U_s \geq U_{s,\min}$$

where

$$U_{s,\min} = I_{k,max,thr} \frac{I_{sn}}{I_{pn}} \left(R_{ct} + R_{wire}\right)$$

In addition to this, the kneepoint voltage must be higher than twice the actual stability voltage:

$$U_{knee} \geq 2 \cdot U_s \qquad \text{(Requirement)}$$

On the other hand, it is not recommended that the knee-point voltage of the CTs is chosen higher than a few times the stabilizing voltage (whereby 4 ..8 times the Uset voltage can be considered as a typical value). This is to prevent over-sizing of auxiliary system elements like resistors and varistors due to their thermal capabilities and overvoltage issues.

$$U_{knee} \leq 8 \cdot U_s \qquad \text{(Guidance value)}$$

where:

U_s:	actual stability voltage
$U_{s,min}$:	minimum stability voltage
U_{knee}:	kneepoint voltage of CT
$I_{k,max,thr}$:	max. symmetrical short-circuit current for external faults
I_{pn}:	CT primary nominal current
I_{sn}:	CT secondary nominal current
R_{ct}:	internal burden of CT
R_{wire}:	cable burden

CALCULATION OF CABLE BURDEN:

The cable burden is calculated by the single length, the cross section, the specific resistivity for copper and an effective factor for the wire length. This factor k_{wire} is 2 if the return wire is to be considered. **Cable burden**:

Length:	l_{wire}	= 150 m
Cross section:	A_{wire}	= 4 mm^2
Spec. resisitivity (Cu):	ρ_{Cu}	= 0.02171 Ω mm^2/m at 75 ^{O}C
Sec. wire current:	$I_{sn,wire}$	= 1 A
Eff. wire length in p.u.:	k_{wire}	= 2

$$R_{wire} = \frac{k_{wire} \cdot \rho_{Cu} \cdot l_{wire}}{A_{wire}}$$ **= 1.6283 Ω**

CHECK OF CT REQUIREMENT:

Calculation of stability voltage:

The minimum stability voltage of SIPROTEC 5 7SJ8x (87B HI) to ensure stability on external faults:

$$U_{s,\min} = I_{k,max,thr} \frac{I_{sn}}{I_{pn}} \left(R_{ct} + R_{wire}\right)$$ = 191.694 V

where:

$U_{s,min}$:	minimum stability voltage	191.694 V
$I_{k,max,thr}$:	max. symmetrical short-circuit current for external faults	63 kA
I_{pn}:	CT primary nominal current	3000 A
I_{sn}:	CT secondary nominal current	1 A
R_{ct}:	internal burden of CT	7.5 Ω
R_{wire}:	cable burden	1.6283 Ω

The actual stability voltage U_S should be set to at least $U_{S,min}$. Based on the chosen current pickup value and the chosen resistor (see below) the effective stability voltage equals to:

U_S = 240 V

Calculation of maximum sensitivity:

The higher the sensitivity, the lower the value of the fault current that is detected by the relay. According to the actual stability voltage and considering that the relay has a variable a.c. current setting of 0.03 A to 100 A in 0.001 A steps, the maximum primary current sensitivity I_p can be obtained:

$$I_p = \frac{I_{pn}}{I_{sn}}\left(I_{s,\min} + N \cdot I_{knee} \cdot \frac{U_s}{U_{knee}} \right) \quad = 210 \text{ A}$$

where:

I_p:	maximum primary current sensitivity	210 A
$I_{s,min}$:	minimum relay current setting	0.05 A
N:	number of CTs in parallel with relay	3
I_{knee}:	mag. current I_{knee} at U_{knee}	0.04 A
U_S:	actual stability voltage	240 V
U_{knee}:	kneepoint voltage of CT	1440 V

This corresponds to a sensitivity of 7% of nominal current of the object I_{n_obj}= 3000 A. This corresponds to a sensitivity of 7% of nominal primary current I_{pn} of the CT.

Desired sensitivity calculation:

For a desired decreased sensitivity of 15 % of I_{n_obj} a corresponding relay current setting can be calculated:

$$I_s = I_{p,des} \cdot \frac{I_{sn}}{I_{pn}} - N \cdot I_{knee} \cdot \frac{U_s}{U_{knee}} \quad = 0.13 \text{ A}$$

where:

I_S:	secondary relay current setting to reach the desired sensitivity	0.13 A
N:	number of CTs in parallel with relay	3
I_{knee}:	mag. Current I_{knee} at U_{knee}	0.04 A
$I_{p,des}$:	desired current sensitivity of object	450 A
U_S:	actual stability voltage	240 V
U_{knee}:	kneepoint voltage of CT	1440 V

Considering the setting range of the relay of 0.03 A to 10 A in 0.001 A steps the pickup current can be chosen:

$I_{s,set}$ = 0.2 A

Effective sensitivity calculation:

The effective sensitivity on the secondary side can be calculated as follows:

$$I_{eff\_sens} = I_{s,set} + N \cdot I_{knee} \cdot \frac{U_s}{U_{knee}} \quad = 0.22 \text{ A}$$

where:

I_{eff_sens}:	effective current sensitivity (secondary)	0.22 A
$I_{s,set}$:	relay current setting	0.2 A
N:	number of CTs in parallel with relay	3
I_{knee}:	mag. current I_{knee} at U_{knee}	0.04 A
U_S:	actual stability voltage	240 V
U_{knee}:	kneepoint voltage of CT	1440 V

This corresponds to a primary fault sensitivity of 660 A (i.e. 22 % of I_{n_obj}= 3000 A). This corresponds to 22% of the primary rated current of the CT I_{pn}=3000 A.

Calculation of stabilizing resistor:

The proper value of stabilizing resistor R_{stab} is required to ensure stability during through-faults and is calculated by using the actual stability voltage = 240 V and the pickup current setting of the relay$I_{s,set}$ = 0.2 A (please refer to above).

$$R_{stab} = \frac{U_s}{I_{s,set}} - R_{relay}$$ = 1200 Ω

where the relay burden R_{relay} = 0.1 Ω is neglected.

The stabilizing resistor R_{stab} can be chosen with a necessary minimum continuous power rating $P_{stab,cont}$ of :

$$P_{stab,cont} \geq \frac{U_s^{\,2}}{R_{stab}}$$ = 48 W

Please note that in order to keep the resistor healthy during commissioning tests the fault current from the testing equipment should be immediately withdrawn after the device gives a protection trip.

Moreover, R_{stab} must have a short time rating large enough to withstand the fault current levels before the fault is cleared. The time duration of 0.5 seconds can be typically considered (P_{stab},0.5s) to take into account longer fault clearance times of back-up protection. The rms voltage developed across the stabilizing resistor is decisive for the thermal stress of the stabilizing resistor. It is calculated according to formula:

$$U_{rms,f} = 1.3 \cdot \sqrt[4]{U_{knee}^{\,3} \cdot R_{stab} \cdot I_{k,\max,\mathrm{int}} \cdot \frac{I_{sn}}{I_{pn}}}$$ = 3828.82 V

where

U_{knee} :	kneepoint voltage of CT	1440 V
R_{stab} :	resistance of the stabilizing resistor	1200 Ω
$I_{k,max,int}$:	max. symmetrical short-circuit current for internal faults	= 63 kA
I_{pn}:	CT primary nominal current	3000 A
I_{sn} :	CT secondary nominal current	1 A

The resulting short-time rating P_{stab},0.5s equals to:

$$P_{stab,0.5s} \geq \frac{U_{rms,f}^{\,2}}{R_{stab}}$$ = 12217 W

Calculation of max. voltage at relay terminal:

The relay should normally be applied with an external varistor which should be connected across the relay and stabilizing resistor input terminals. The varistor limits the voltage across the terminals under maximum internal fault conditions. The theoretical rms voltage which may occur across the panel terminals (i.e. tie with relay and R_{stab} connected in series) can be determined according to the following equation:

$$U_{k,\max,\mathrm{int}} = I_{k,\max,\mathrm{int}} \cdot \frac{I_{sn}}{I_{pn}} \cdot \left(R_{relay} + R_{stab}\right)$$ = 25200 V

where the relay burden R_{relay} = 0.05 Ω is neglected.

The resulting maximum peak voltage across the panel terminals (i.e. tie with relay and R_{stab} connected in series):

$$U_{max,relay} = 2\sqrt{2U_{knee}(U_{k,max,int} - U_{knee})}$$ = 16544 V

where:

$I_{k, max, int}$:	max. symmetrical short-circuit current of internal faults	= 63 kA

CT dimensioning check:

Requirement:

The minimum kneepoint voltage of the CTs must be twice the relay setting voltage

$$U_{knee} \geq 2 \cdot U_s$$

U_{knee}	= 1440 V	
2 U_S	= 480 V	Meets requirement

Recommendation:

Furthermore, it is recommended that the kneepoint voltage of the CT should not be higher than eight times the relay setting voltage.

$$U_{knee} \leq 8 \cdot U_s$$

U_{knee}	= 1440 V	
8 U_S	= 1920 V	Meets the recommendation

CTs correctly dimensioned

Varistor check:

A varistor is required if:

$U_{max,relay}$ ≥1500 V

In this case:

$U_{max,relay}$ = 16544 V

Varistor required

E.g. in this case a Metrosil of type 600A/S1/1088 can be used.

1.6.3 Relay sensitivity and speed at internal faults (in detail)

1.6.3.1 Examples for internal fault tests

The relay was subjected to numerous tests with regard to the speed on internal faults observing it for each of the overcurrent elements (fundamental, true RMS and instantaneous).

EXAMPLE 1I (no saturation) As an Example 1 in Figure 12 a scheme for internal resistive fault is shown. The example presents a primary fault current of 3.4kA magnitude (which corresponds to approx. 5 times setting value $I_{fault}/I_{p,des}$) for the case utilizing CTs with E_k / U_{set} =4.

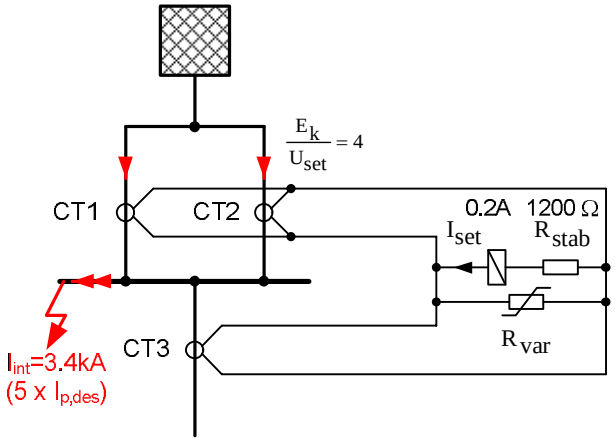


Figure 12 Scheme for an internal fault with simulated quantities, example 1I

In practice this could be a resistive fault on a busbar. Therefore, only very small or no decaying DC component is available for such kind of fault (Figure 13).

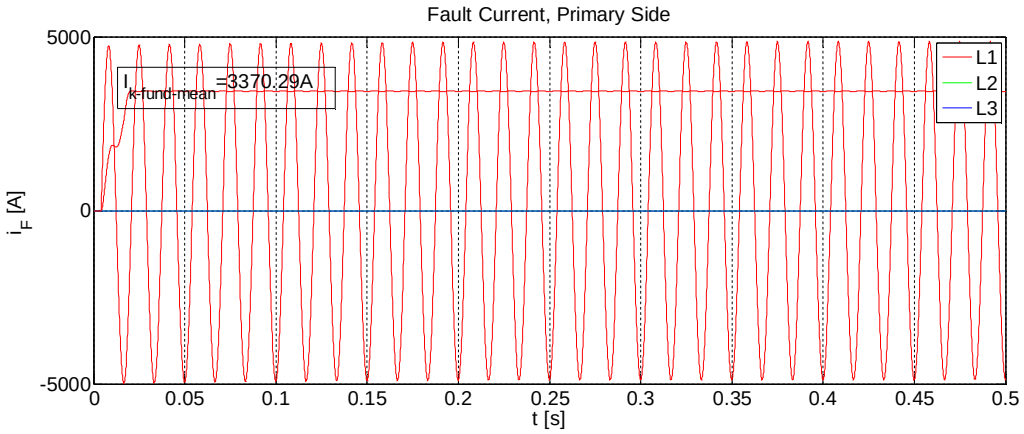


Figure 13 Primary fault current for an internal fault without decaying DC-component, example 1I

The resulting differential current that flows in the differential tie and so through the relay is shown in following figure. The shape of this differential current is quite sinusoidal, as the fault current is not so high, so the CTs within the scheme (all CTs are connected in parallel, CT3 observes no primary current) can equalize itself almost within its linear area. The reaction of the relay on such fault current will be typically very predictable, as the curve is almost sinusoidal.

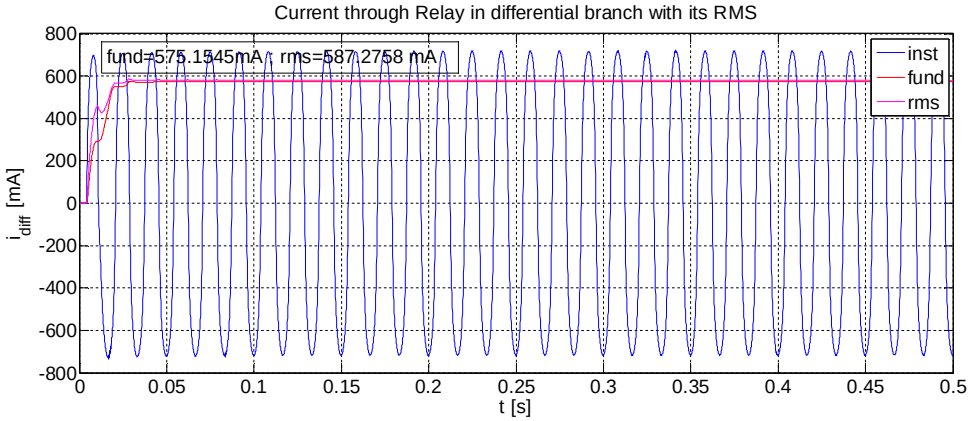


Figure 14 Differential current as it will be seen by the relay, example 1I

As a further example (Example 2I) a strong internal fault (e.g. metallic with no fault resistance) with current magnitude of 63kA primary is then shown in Figure 15 and Figure 16, respectively. Practically it corresponds to very severe metallic fault at the busbar, which is very rare, but not impossible. The reaction of the relay on such a fault shall be very fast.

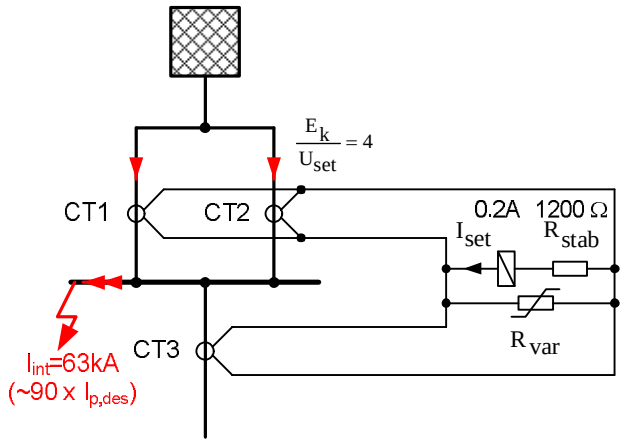


Figure 15 Scheme for an internal fault with simulated quantities, example 2I

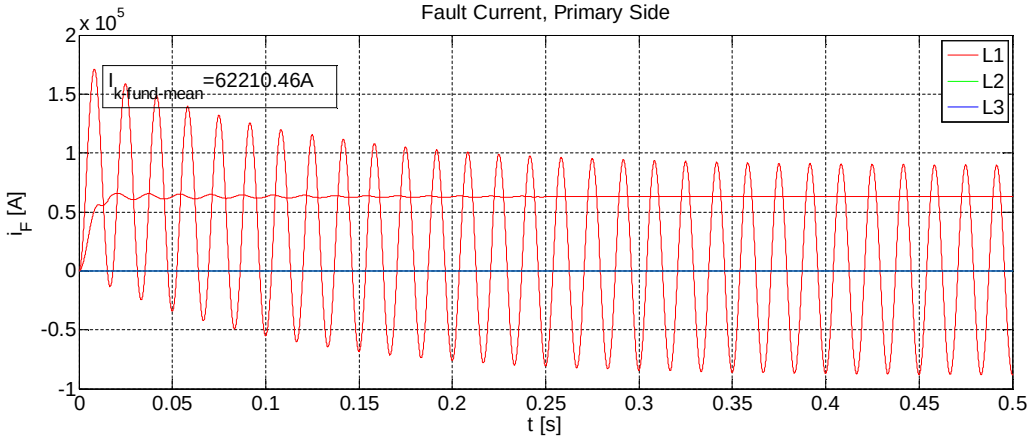


Figure 16 Primary fault current for an internal fault with decaying DC-component, example 2I

The current in the differential branch is strongly distorted, as in such cases the CTs fully run their magnetizing characteristic (trying to equalize itself within the scheme) and developing high voltages (that actually depend on their E_k). The presence of varistor protects the secondary circuit from overvoltages (Figure 18). As the current curve is very steep the reaction of the used overcurrent elements shall be fast, with slight differences between them.

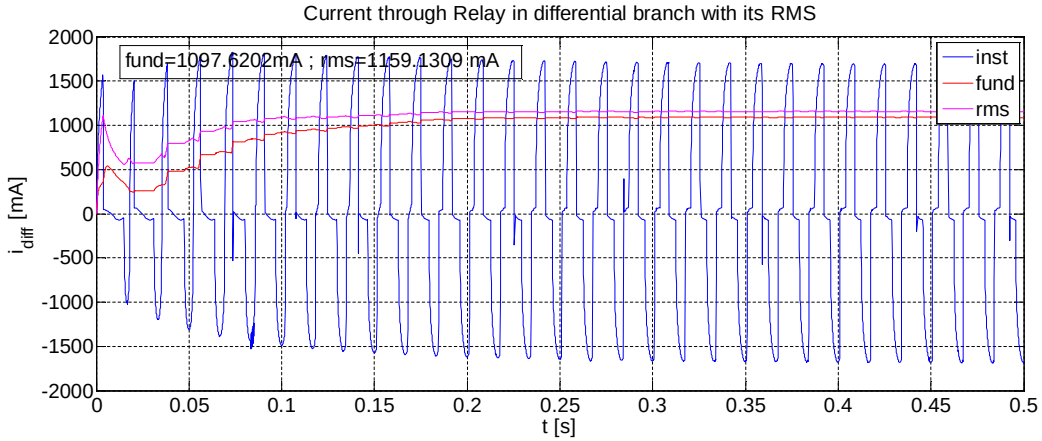
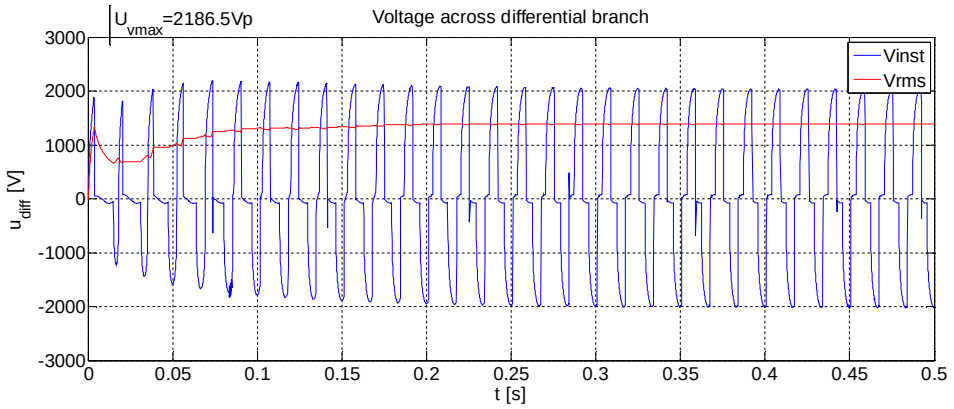


Figure 17 Differential current as it will be seen by the relay, example 2I

(a)



(b)

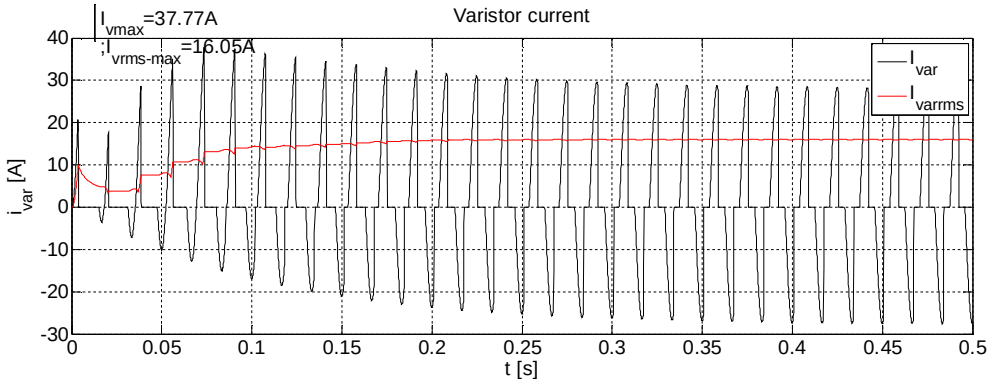


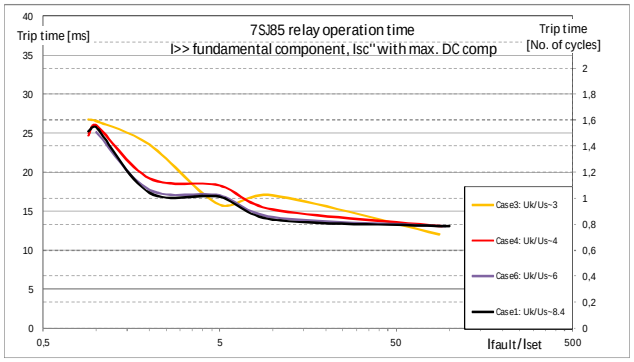
Figure 18 Voltage across the differential branch (a) and the varistor current (b) , example 2I

1.6.3.2 Summarized results of internal fault tests

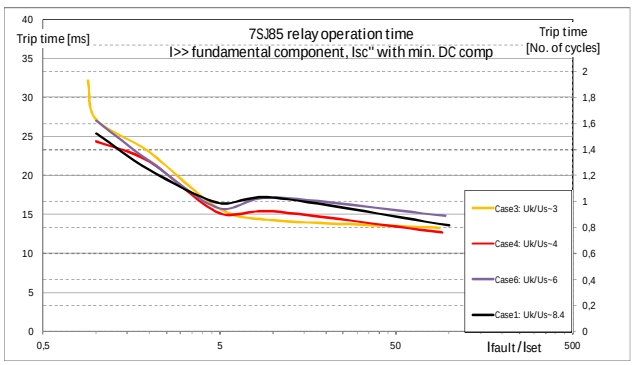
As a summary, in following the tripping times for the three tested elements (fundamental, true RMS and instantaneous) are shown as a function of fault sensitivity for different scheme configuration cases. Each of the figures show tripping time (shown on Y-axis: left in ms, right as a relation to the period time) for various E_k / U_{set} ratios (shown as Uk/Us lines with different colours). The primary fault current was modified to reach various primary fault current/ scheme fault sensitivity ratios $I_{fault} / I_{p,des}$ (shown as Ifault/Iset on X-axis).

Figure 19 presents the summary of the total tripping times (including trip relay) as tested for all the cases.

maximum decaying DC component in the current: (MAX DC)



symmetrical short-circuit current: (MIN DC)



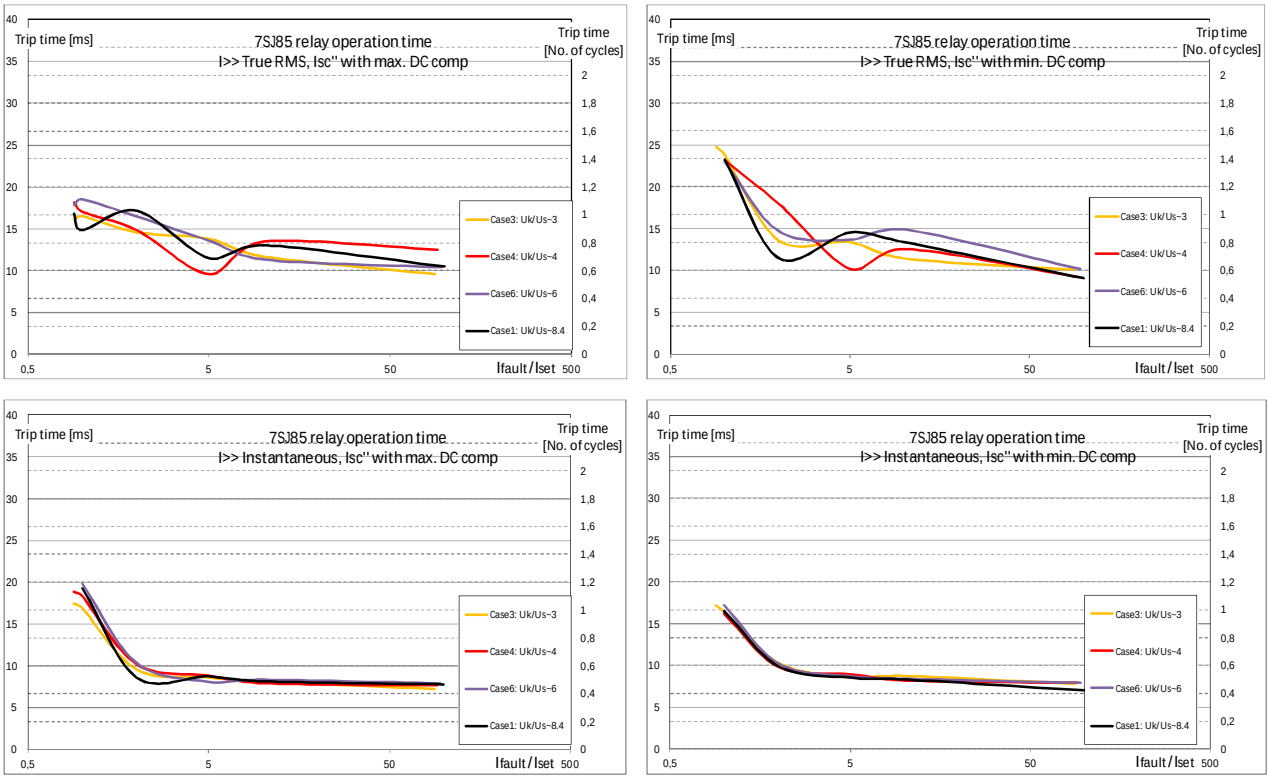


Figure 19 Summarized results of the relay speed tests at internal faults 87BHI tests (60Hz)

For typical scheme design with E_k / U_{set} in the range of 3 to 6 one can observe that the typical trip time of the relay lies in the range of 0.6 – 0.8 times the cycle duration (i.e. for 60Hz and fundamental element used it results with 0.8 times 16ms=approx. 12ms).
The shortest trip time in the range of 7ms (at approx. 0.5 of cycle duration at 60Hz) can be observed for the maximum fault currents and usage of instantaneous element.

1.6.3.3 Contact time (internal device trip/ trip on contact)

The contact time of the relay was observed, as well. It was calculated subtracting the reading form the Omicron (device trip on binary output contact) from the reading made in the respective fault recording (DIGSI) for every case tested. Figure 20 shows these readings together with the resulted contact time for an exemplarily chosen case.

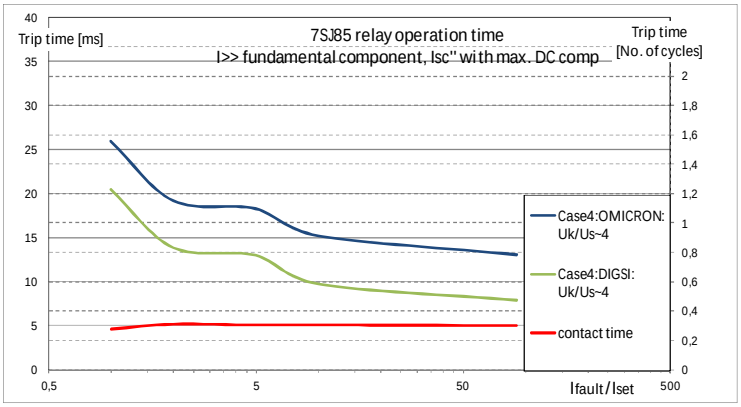


Figure 20 Exemplary results of testing showing determination of the relay tripping contact time

Summarizing, the average contact time of approx. 5ms was observed. The spreading was less than 0.2ms so below the metering accuracy. Since the tested relay SIPROTEC 5 7SJ85 utilized fast tripping contacts (type F), the resulting average contact time of around 5ms was in line with the relay manual.

1.6.3.4 Relay speed on internal faults: summary

As a summary, one can state that using fundamental element together with Fast Tripping Relay (type F) brings already satisfactory results regarding tripping time. The usage of High-Speed Relay with Semiconductor Acceleration (Type HS) will reduce the overall tripping time to values well below ½ Period (below 10ms). Figure 21 shows the summarized results of the relay overall tripping speed at internal faults using fundamental component element and two mentioned types of contacts, respectively.

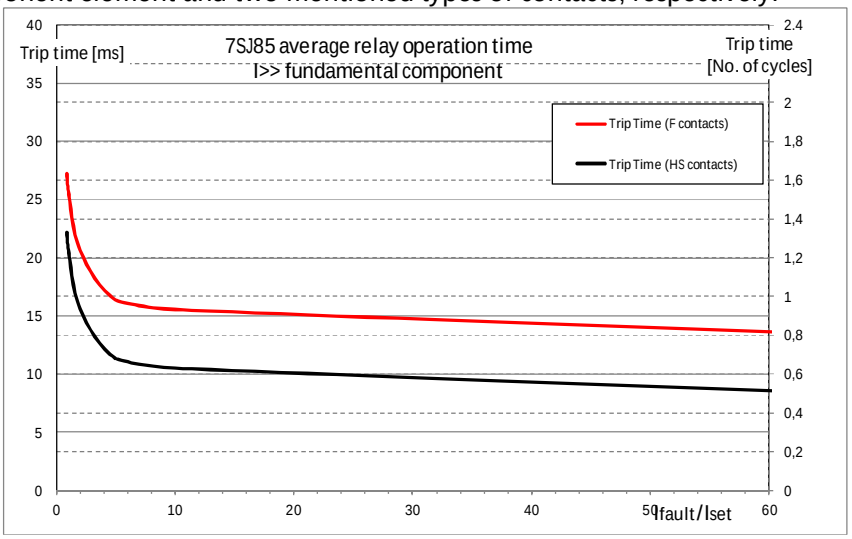


Figure 21 Summarized trip time curve for all cases tested, fundamental component (60Hz 87B HI)

For the sake of complicity the summarized tripping times for the true RMS and instantaneous elements are shown in Figure 22.

The tripping time of the other elements, especially the instantaneous element is shorter. However, the usage of those elements is not proposed for 87B HI, since their stability on external faults is not optimal, as the tests with external faults showed (see remarks in the following chapter).

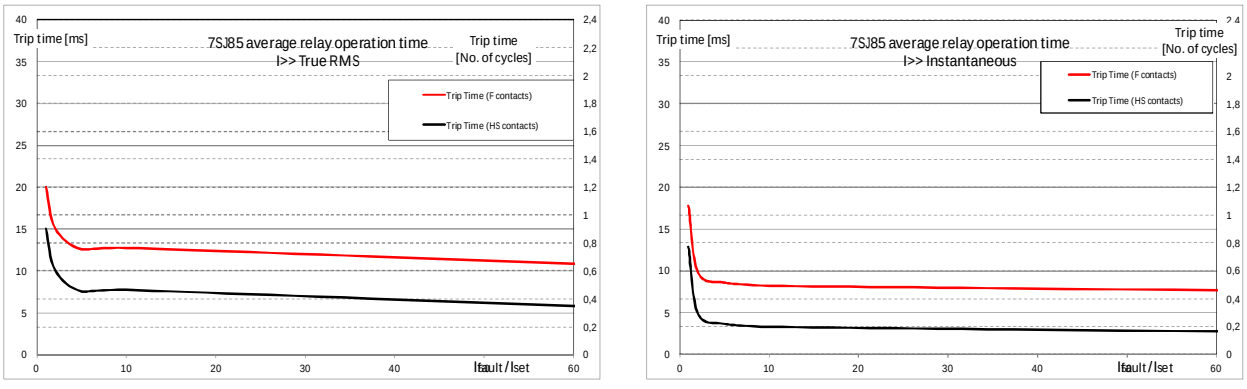


Figure 22 Summarized trip time curve for all cases tested true RMS, instantaneous (60Hz 87B HI)

1.6.4 Relay stability at external faults

For busbar protection schemes it is essential to keep the scheme stable during external faults, especially those close-in metallic faults at the outgoing feeder (like those just behind the outgoing feeder CTs). Thereby, the scheme shall remain stable in all the practical conditions. Among others, the latest include:

- Slightly unequal CT parameters in terms of:
  - CT Ratio, $k_r = \frac{I_{pr}}{I_{sr}}$, respectively with the maximum possible turns ratio error for the IEC Class PX of 0.25%,
  - Rated CT knee-point emf E_k, (in steps of -10%, -20% ,-30%, ..)
  - CT exciting current at the knee-point emf I_e (in steps of +10%, +20% , +30%, ..)
  - CT secondary winding resistance R_{CT} (in steps of +10%, +20% , +30%, ..)
- Unequal secondary wiring lengths R_{wire} (in steps of +10%, +20% , +30%, ..)

Moreover, in practice, some of the CTs could have remanence flux at the fault inception, therefore also cases with remanence of the CTs were considered, as well.

The mentioned conditions were then included in the tested cases. Thereby, all three overcurrent stages utilizing fundamental, true rms and instantaneous measurement method were tested on their stability during external fault conditions.

In Figure 23 the external faults scheme is shown. Thereby, in order to represent the worst case, CT3 was subjected to the a.m. changes.

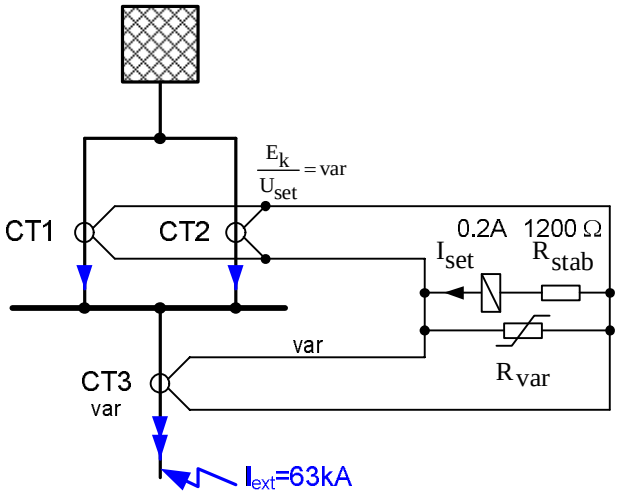


Figure 23 Scheme for external faults simulations and tests

Below, some chosen examples of the tested cases are presented.

EXAMPLE 1E: CASE 6 (E_k / U_{set} =6) EXT FAULT max DC, all CTs equal

In Figure 24 a primary fault current in phase L1 is shown (63kA). The fault inception is close to the respective voltage zero crossing so that the maximum decaying DC component can be observed. The calculated curve of the respective fundamental component rms is shown only for information. The fault is an external one, as per Figure 23.

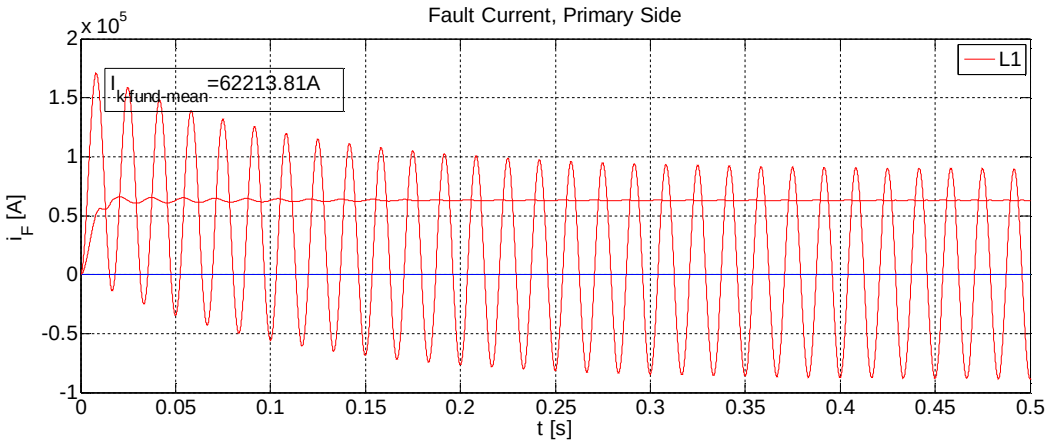


Figure 24 Primary fault current (external) shown only for phase L1, EXAMPLE 1E

The magnetic flux course within the CTs in the scheme is shown in Figure 25.

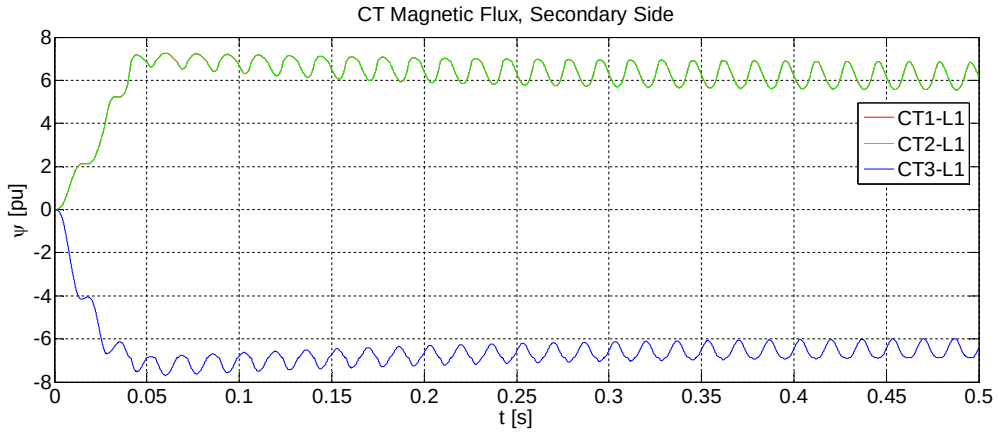


Figure 25 CTs flux course during the fault (red curve lies directly below green one), EXAMPLE 1E

Because the CT1 and CT2 are assumed to be identical the CT1 (red) flux course lies directly below the CT2 (green) and cannot be seen in this figure. The CT3 (outgoing feeder CT) shall equalize the scheme, but mainly due to the higher current (full short circuit current flows through CT2, while CT1 and CT2 observe only halve of it) and its DC component, the saturation is reached at ~ 25ms, while the other two CTs saturate later. This results in a higher differential current, as can be seen in Figure 26.

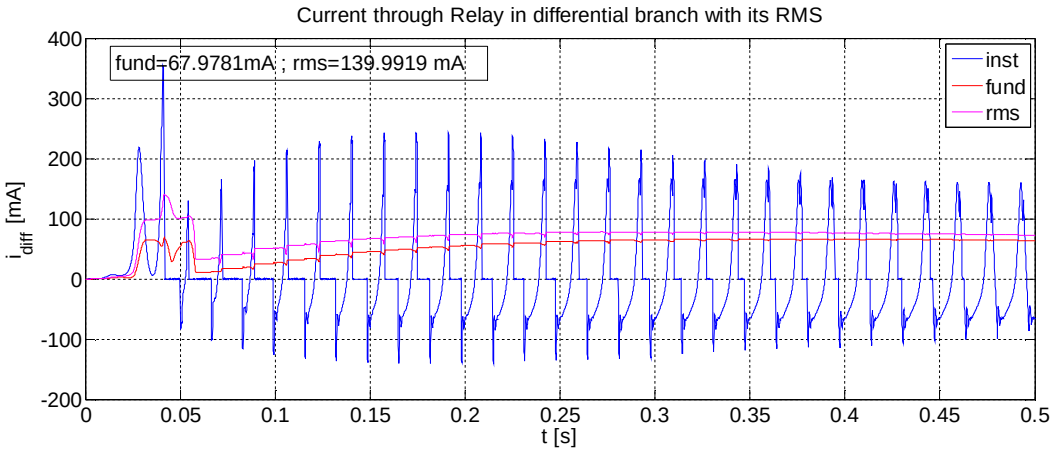


Figure 26 Resulting differential current (as it will be seen by the relay), EXAMPLE 1E

This differential current increase may already lead to the trip of the instantaneous element (instantaneous curve lies above the threshold of 200*sqrt(2) mA), but the tested relay remains stable.

Further increasing of scheme irregularity, however, leads to operation of the relay on external faults (mainly by instantaneous, but also by true rms elements), as it will be shown in examples below.

EXAMPLE 2E: CASE 6 (as Example 1E, but CT3 has 10% deviation (E_k , I_e , R_{CT} , R_{wire} and turns ratio error of 0.25% of CT3)

For the same primary fault current, as in Figure 24 the CTs flux course is shown in Figure 27 .

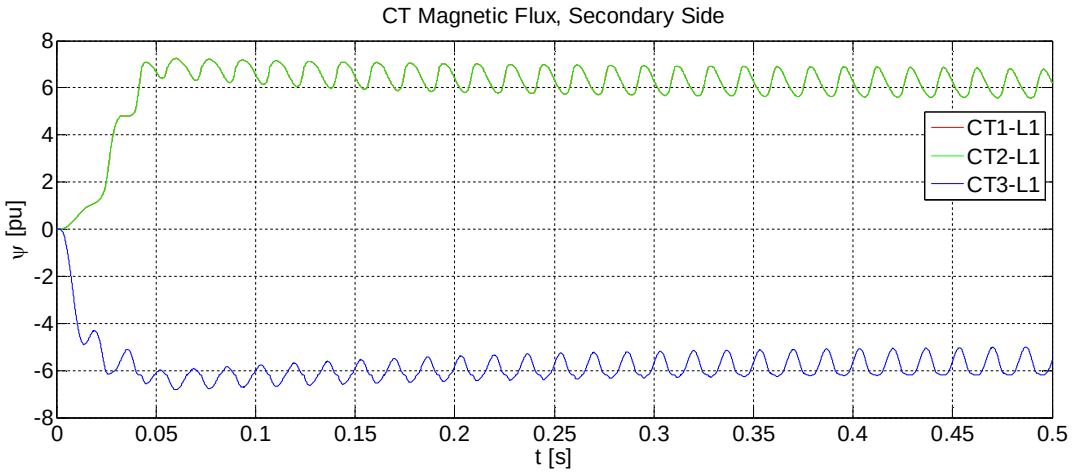


Figure 27 CTs flux course during the fault (red curve lies directly below green one), EXAMPLE 2E

Because the CT1 and CT2 are assumed to be identical the CT1 (red) flux course lies directly below the CT2 (green) and cannot be seen in this figure. The CT3 (outgoing feeder CT) has now 10% deviation within the parameters (as indicated above). Due to smaller knee-point emf, the CT3 flux curse is now different than in Figure 25, so the resulting current in the differential branch increases. The resulting current in the differential branch, as it will be seen by the relay is shown in Figure 28.

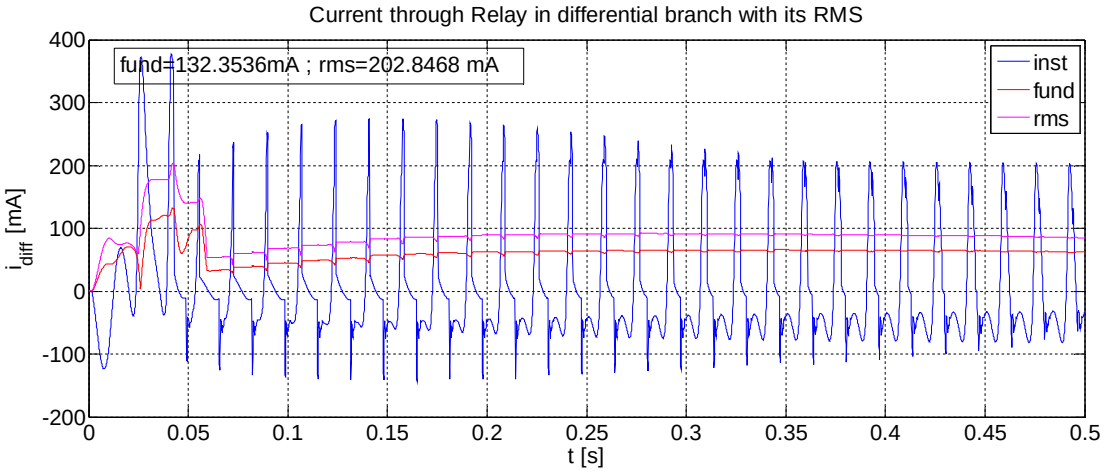


Figure 28 Resulting differential current (as it will be seen by the relay), EXAMPLE 2E

The relay trips using instantaneous measuring method. In Figure 29 the respective trip record form the relay is shown.

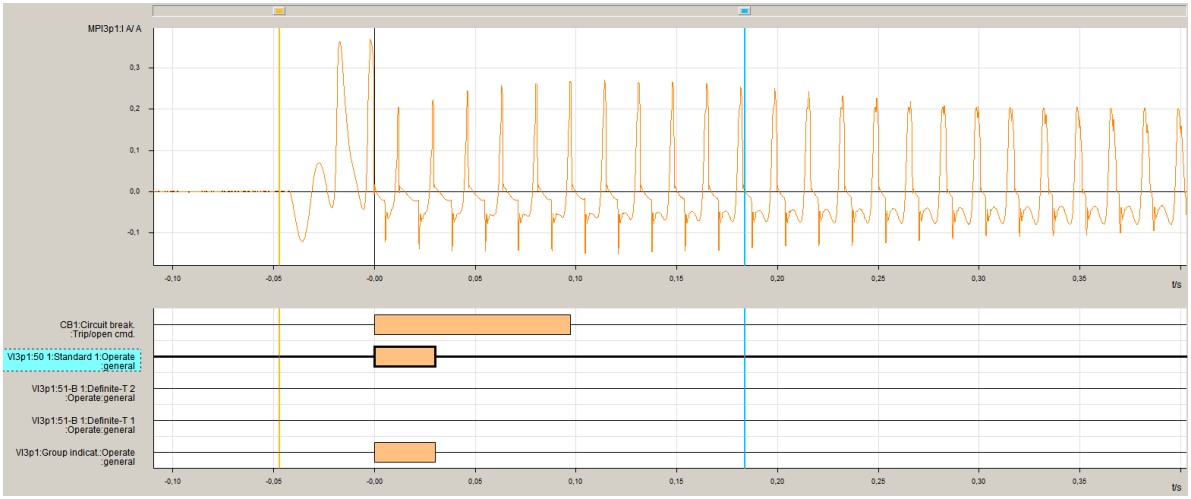


Figure 29 Trip record read from the relay (Case 6 CT3 all its parameter have 10% dev, DIGSI flt. Nr. 176), EXAMPLE 2E

REMARK: Description of SIGRA binary signals shown in SIGRA drawings within this document is as follows:
Circuit Breaker trip command = General trip
VI3p1:50 1: Standard 1: Operate General = Instantaneous element
VI3p1:51- B 1: Definite T2 = True RMS element
VI3p1:51- B 1: Definite T1 = Fundamental element

One can observe that in this case the first 40-50 ms seem to be most problematic for the instantaneous element. The primary fault current due to its transient DC component leads to steep increase of the flux magnetic of the CTs. As a consequence of slightly unequal secondary circuit parameters (CT3 as well as its respective wiring deviate by approx. 10% from the other CT1&2) the CT equalization varies from the ideal conditions. As a result, the higher current in the differential branch appears that leads to trip of the Instantaneous element (VI3p1:50 1: Standard 1: Operate General) of the relay. The fundamental component (VI3p1:51- B 1: Definite T1) and true RMS (VI3p1:51- B 1: Definite T2) remain stable.

EXAMPLE 3E: CASE 6 (E_k / U_{set} =6) same CT parameter, but CT3 has initial remanence flux (~80%)

As a next example, a further realistic case where CTs within the scheme have slightly different parameters (CT3 deviate by 10% form the other ones, as in examples above) and now this CT core has an initial remanence flux of approx. 90% of the saturation flux. The primary external fault of 63kA comes with DC component (as in Figure 24). The respective flux course within the CTs can be observed in Figure 30.

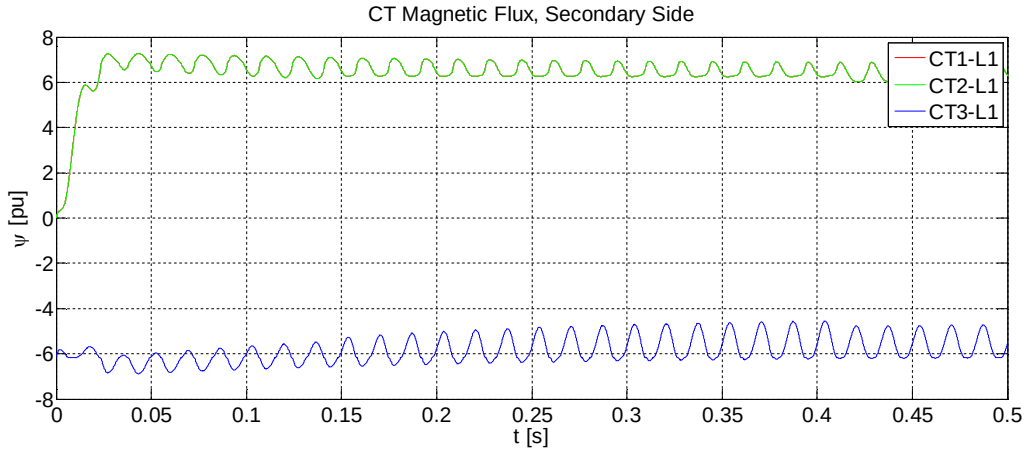


Figure 30 CTs flux course during the fault (red curve lies directly below green one), EXAMPLE 3E

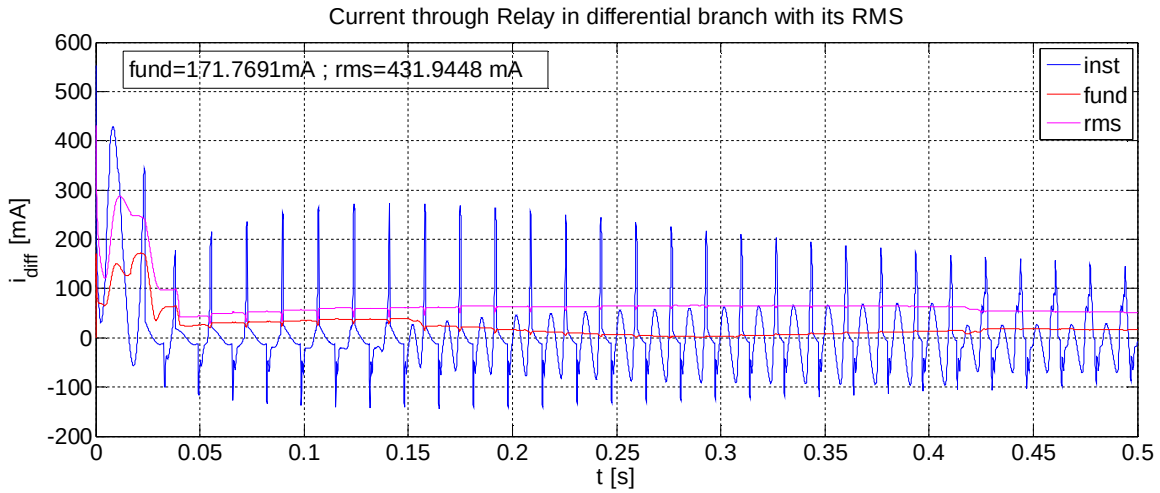


Figure 31 Resulting differential current (as it will be seen by the relay), EXAMPLE 3E

Using instantaneous and true rms measuring method the relay trips. In Figure 32 the respective trip record form the relay is shown.

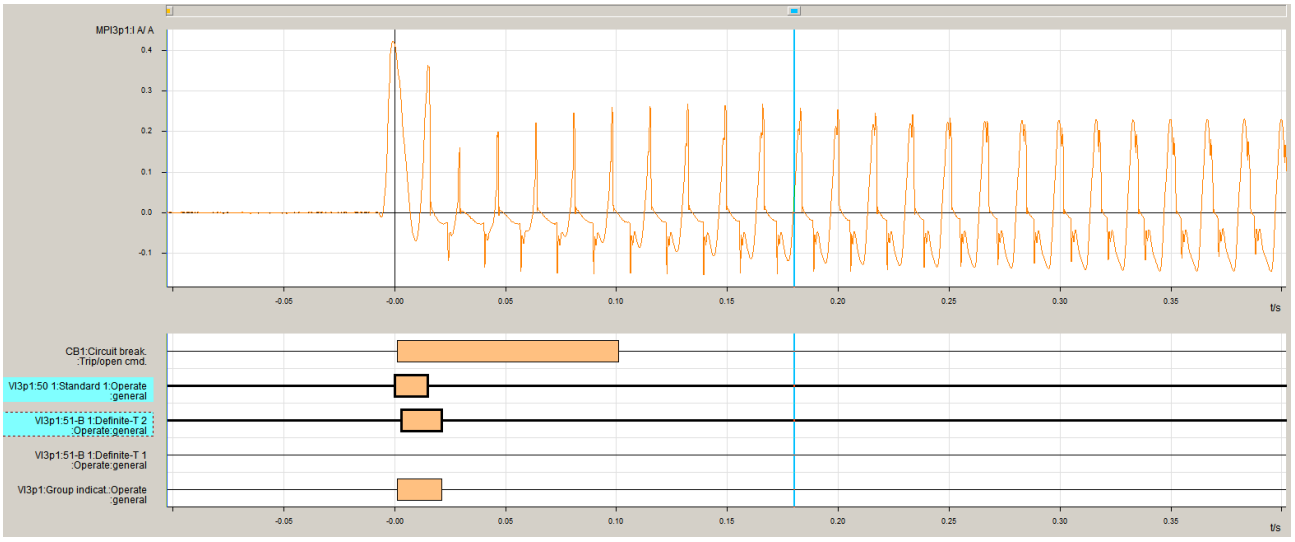
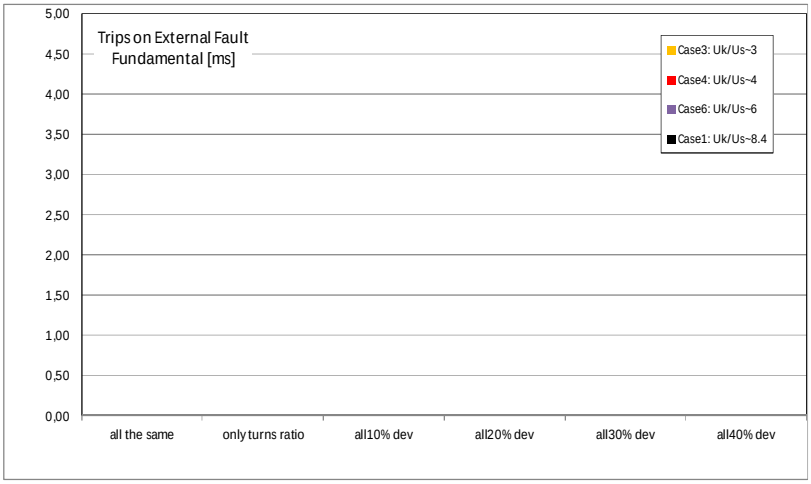
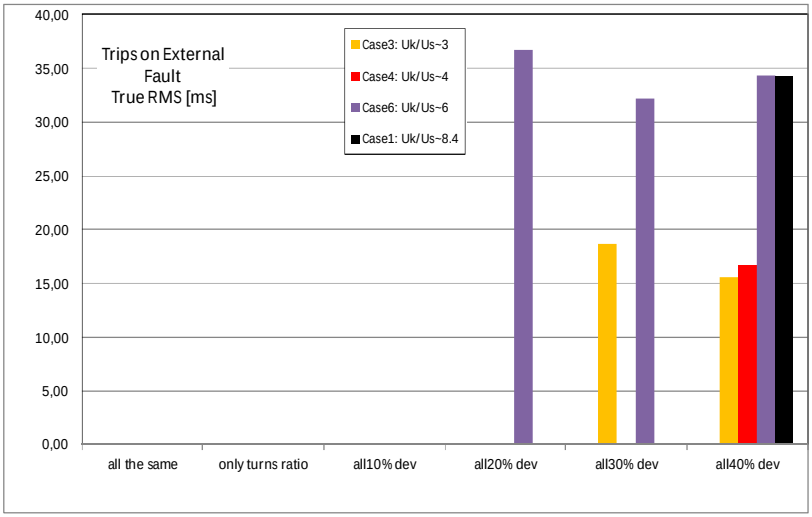


Figure 32 Trip record read from the relay (CT3 has remanence and all its parameters vary by 10%; Case 6, DIGSI flt. Nr. 201), EXAMPLE 3E

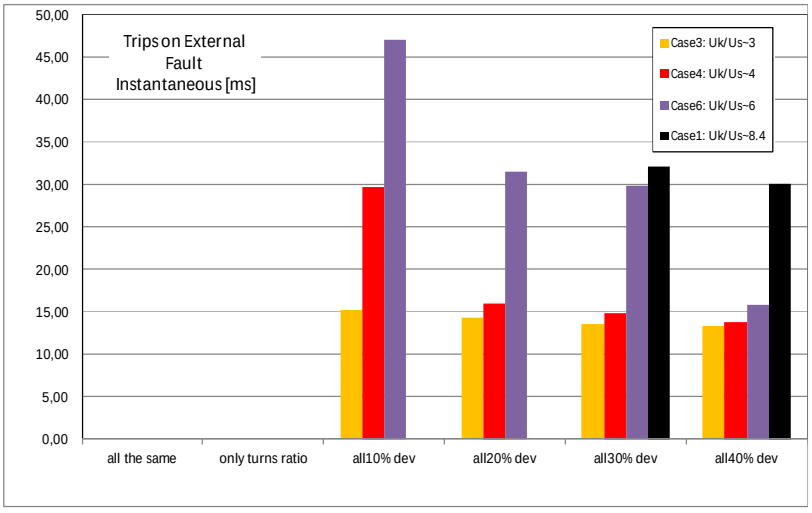
In following figure the summary of the external fault tests is presented. Thereby, the tripping time shown on the y-axis plays minor role, rather than the trip at all, as the requirement is to remain stable on external faults



fundamental element



true RMS elemnt



instantaneous element

Figure 33 Tripping on external fault; Summary of the tested cases

As one can observe, the fundamental element has the optimal stability throughout all the tested cases. No overfunction took place, as it was the case with true rms and instantaneous value measurement.

For the test with 50Hz schemes for internal and external faults comparable results were achieved. The overall summary is presented in the next chapter.

1.7 Summary for usage of SIPROTEC 7SJ8x relay as 87B HI

Numerous tests on relay stability on external (through) fault current have shown that multifunctional relay SIPROTEC 5 7SJ8x using proposed overcurrent element (fundamental component) remains stable, even in cases when the high impedance protection scheme reaches considerable level of deviation of scheme parameters (i.e. max. turns ratio error and deviation of connected wiring resistances and all other CT nameplate parameters by more than 40%).
This shall cover all practical cases, as typically the deviation level in real schemes is smaller.

Since some deviation cannot be avoided in practical schemes, the usage of the other elements (true RMS, instantaneous element) is not recommended for 87B HI application.

1.7.1 Generalized curve showing tripping times vs. fault setting

The curves in Figure 34 show average tripping time of all the tested internal faults (50Hz and 60Hz) in relation to the period duration. The total relay operation time using fast contacts (standard) as well high speed contacts is shown, as well.

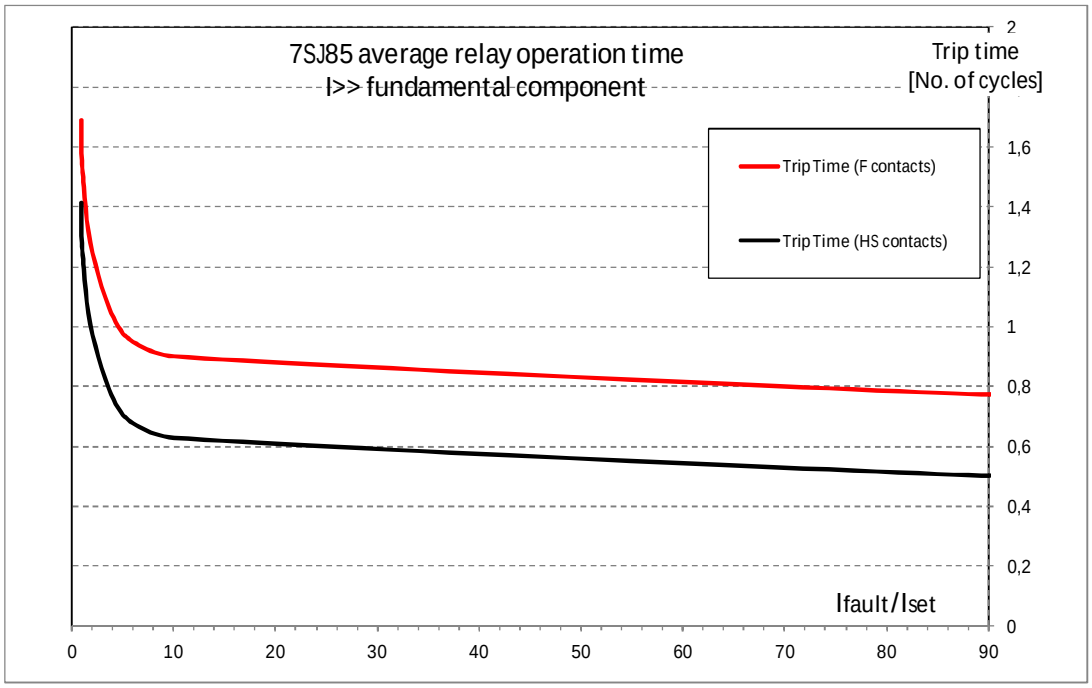


Figure 34 Relay operating time (using fundamental element) for internal faults

In Figure 35 the zoom of curves from Figure 34 for the region of small ratios $I_{fault}/I_{p,des}$ (smaller fault currents) is shown.

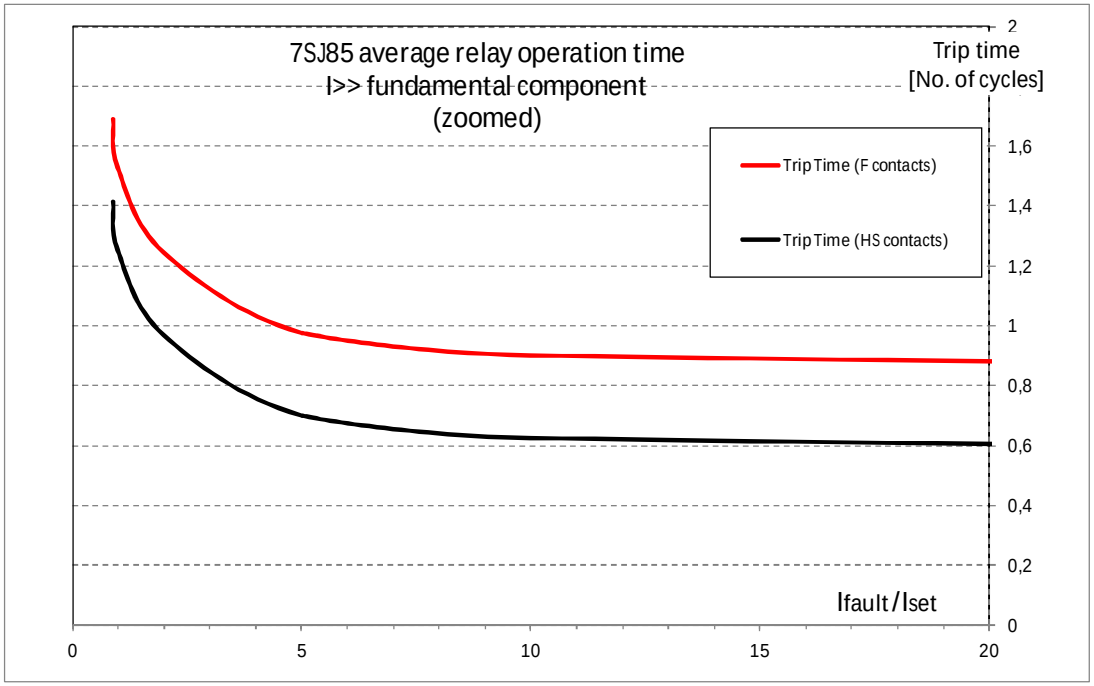


Figure 35 Relay operating time (using fundamental element) for internal faults (Figure 34 zoomed)

1.8 References

[1] International Standard IEC 61869-2, Edition 1.0, 2012-09, Instrument Transformers – Part.2: Additional requirements for current transformers

[2] ENA Energy Network association: Technical Specification 48-3, Issue 2 2013, Instantaneous high-impedance differential protection

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